VocalFusion Stereo Dev Kit for Amazon AVS Hardware Manual

IN THIS DOCUMENT

The **VocalFusion Stereo Dev Kit for Amazon AVS** is an application specific design for far-field voice capture and processing, targeted at Amazon Alexa Voice Service (AVS) applications.

The kit is based on the XVF3500 voice processor and includes:

- linear array of 4 omni-directional microphones: up to 180° capture, for 'edge of the room' applications
- low-jitter audio clock
- configurable user input buttons and LEDs
- I2S audio and I2C control connectivity
- USB powered, with optional USB2.0 device audio and control connectivity

The XVF3500 on the kit is pre-flashed with a software image that implements the VocalFusion Stereo microphone capture and voice processing library, audio and control connectivity, user interfaces and system control.

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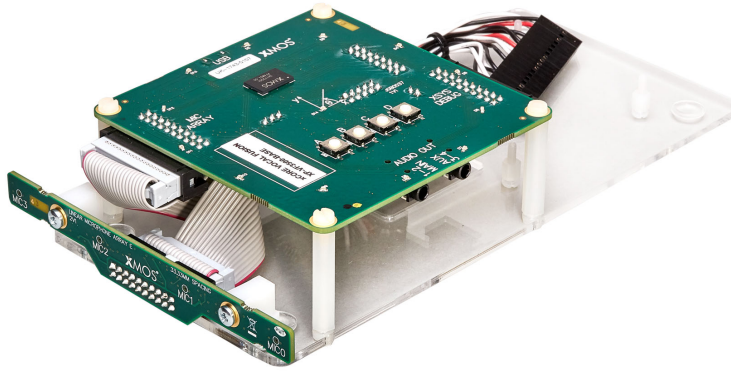

Figure 1: VocalFusion Stereo Dev Kit for Amazon AVS

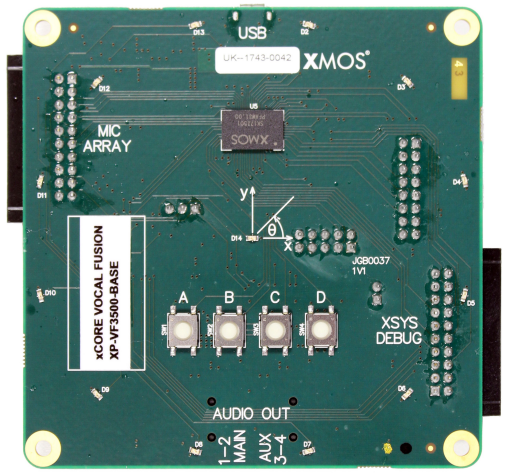

Figure 2: VocalFusion XVF3500 BaseBoard

Figure 3: VocalFusion Linear Microphone board

1 Features

The VocalFusion Stereo Dev Kit for Amazon AVS block diagram is shown in Figure 4 below. It includes:

- VocalFusion XVF3500 Voice Processor
- Four MEMS microphones on a separate board
- A micro-USB connector for power (and optionally USB2.0 device connectivity)
- Extension headers for I2S audio and I2C control connectivity
- Four general purpose push-button switches
- 13 user-controlled LEDs
- Low-jitter clock source
- An xSYS connector for an xTAG debug adapter

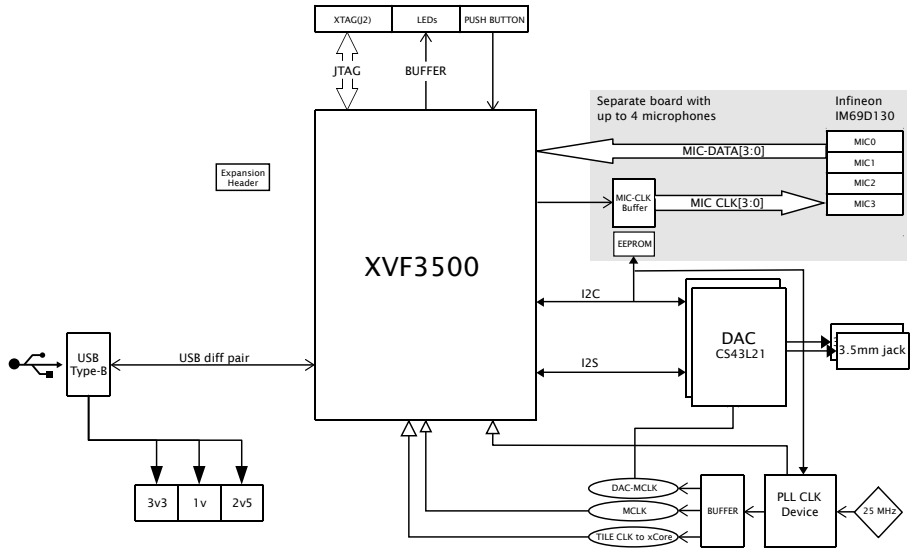

Figure 4: VocalFusion Stereo Dev Kit for Amazon AVS block diagram

2 Introduction

The VocalFusion Stereo Dev Kit for Amazon AVS (XK-VF3500-L33-AVS), Figure 1) consists of a VocalFusion XVF3500 BaseBoard (XP-VF3500-BASE), Figure 2) and separate linear microphone array (LINEAR MICROPHONE ARRAY E, Figure 3) using Infineon IM69D130[1] MEMS microphones.

The VocalFusion BaseBoard is based on the XVF3500 device, running software which integrates the VocalFusion microphone capture and voice processing library providing: beamforming, Stereo Acoustic Echo Cancellation (AEC), noise suppression, de-reverberation and Automatic Gain Control (AGC).

The XVF3500 device has 32 32-bit logical processing cores and is available in a small footprint FB167 package.

For device specific information on the XVF3500 device see the XVF3500 Datasheet[2]. For general information on XVF and xCORE-200 devices see the xCORE-200 Architecture Overview[3].

[1] http://www.infineon.com/microphones
[2] http://www.xmos.com/published/xvf3500-fb167-datasheet
[3] http://www.xmos.com/published/xcore-architecture

3 Clock Sources and Distribution

The VocalFusion XVF3500 BaseBoard includes a single clock generator (Si5351A-B04486-GT, U25, see Figure 5 below) that generates two clocks:

- XVF3500 reference clock - 24MHz oscillator
- Low jitter master clock - 24.576MHz oscillator, used for the DACs and (indirectly) the microphones

The clock generator is controlled by the XVF3500 over the I2C bus (see §6 below).

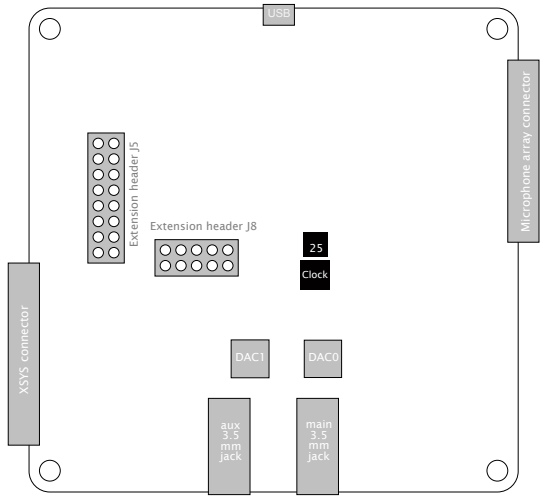

Figure 5: Clock and oscillator locations

4 Stereo DAC with Headphone Amplifier

A CS43L21 stereo DAC with integrated headphone amplifier (DAC0) is used to generate stereo audio output on a 3.5mm audio jack, see Figure 6. A second CS43L21 (DAC1) can be used for auxiliary purposes on a secondary 3.5mm audio jack.

The CS43L21 devices are connected to the XVF3500 device through an I2S interface and are configured using the I2C bus (see §6 below).

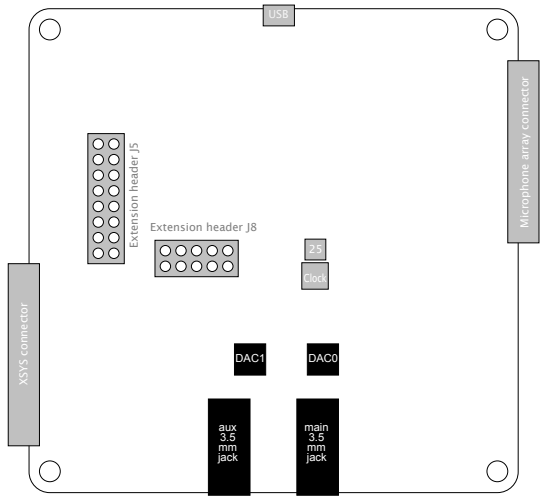

Figure 6: Locations of DACs and 3.5mm audio jacks

The I2S interfaces of the CS43L21 stereo DAC/HPA devices are connected to the XVF3500 GPIO pins as shown in Figure 7 below. They share all signals except for the reset and data lines.

Pin	Port	Signal
X2D22	P1G0	MCLK_TILE0
X2D25	P1J0	I2S_DAC1_DATA
X2D32	P4E2	DAC0_RST_N
X2D33	P4E3	DAC1_RST_N
X2D34	P1K0	I2S_DAC0_DATA
X2D35	P1L0	I2S_LRCK
X2D36	P1M0	I2S_BCLK

Figure 7: Stereo DAC GPIO pins

5 MEMS Microphone Boards

The microphone board is plugged into connector J3 on the VocalFusion XVF3500 BaseBoard using a ribbon cable (see Figure 8). A short ribbon cable should be used for signal integrity.

The microphones should **not** be plugged into the xSYS connector.

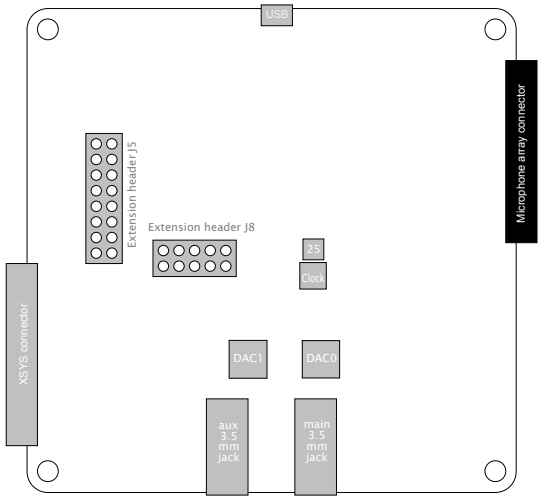

Figure 8: Microphone connector location

The microphone array consists of a linear array of four microphones, spaced 33.33mm apart, a clock buffer, and an EEPROM for optional identification.

The microphone signals are mapped onto the XVF3500 device as show in Figure 9.

Microphone	GPIO	Port
MIC_0	X2D14	P8B0
MIC_1	X2D15	P8B1
MIC_2	X2D16	P8B2
MIC_3	X2D17	P8B3
MCLK_IN	X2D22	P1G0
MIC_CLK	X2D23	P1H0

Figure 9: Linear MEMS microphone board GPIO pins

6 I2C Bus

The VocalFusion XVF3500 BaseBoard has a main I2C bus that is used to control the DACs, clock generator, and EEPROM. This main I2C bus is connected to tile 2 of the XVF3500, with the XVF3500 acting as a master on the I2C bus. See Figure 10 below.

Figure 10: I2C master GPIO pins

Pin	Port	Signal
X2D28	P4F0	I2C_SCL
X2D29	P4F1	I2C_SDA

The addresses of devices on the I2C bus are shown in Figure 11 below.

Figure 11: I2C device addresses

Device	Sch ID	Address	
Si5351A (Clock)	U25	0b1100010	0x62
CS43L21 (DAC0)	U23	0b1001010	0x4A
CS43L21 (DAC1, aux)	U9	0b1001010	0x4B
24LC08B (EEPROM on microphone board)	U5	0b1010xxx	0x5x

Please refer to the 24LC08B datasheet for details on how to address the EEPROM.

The VocalFusion XVF3500 BaseBoard also has a secondary I2C bus, on which the XVF3500 is a slave. This allows the XVF3500 to be controlled by an external I2C host. See Figure 12 below.

Figure 12: I2C slave GPIO pins

GPIO pin	Port	Signal
X0D36	P1M0	I2C_SCL_EXT
X0D37	P1N1	I2C_SDA_EXT

This slave I2C interface is wired up to the extension headers (see §8).

7 General Purpose User Interface

The VocalFusion XVF3500 BaseBoard has 13 LEDs that are controlled by two 74HC595 LED drivers. LED_0 - LED_11 (D2-D13) are positioned around the edge of the board, one each side of every microphone. LED_12 (D14) is positioned next to the middle microphone. The LEDs are driven by serially clocking data into the 16-bit shift register that is formed by the two drivers. The top three bits of the shift register are not used, the other 13 drive the LEDs. A '0' should be shifted in to drive a LED.

Four general purpose push-button switches are provided. When pressed, each button creates a connection from the I/O to GND. To ensure correct behaviour, the port connected to the buttons (P4F) must always be defined as an input.

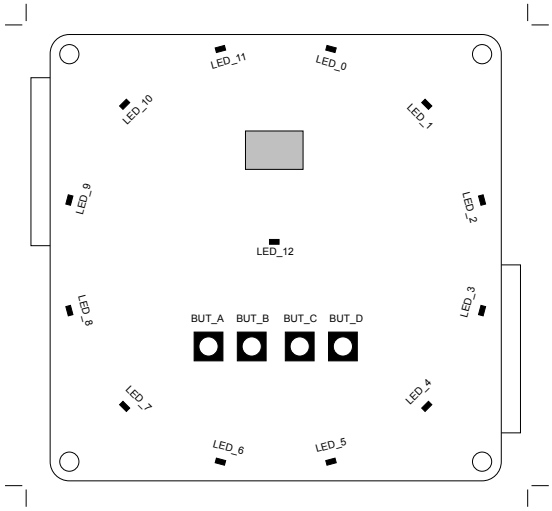

Figure 13: General purpose user interface components

The signal mapping of the user interface components to the XVF3500 GPIO is shown in Figure 14 and Figure 15

UI signal	GPIO pin	Port
BUTTON_A	X0D28	P4F0
BUTTON_B	X0D29	P4F1
BUTTON_C	X0D30	P4F2
BUTTON_D	X0D31	P4F3

Figure 14: User interface GPIO

UI signal	GPIO pin	Port	Notes
LED_STCP	X3D00	P1A0	Connects to Store/Latch clock on LED driver
LED_SHCP	X3D01	P1B0	Connects to Shift Clock on LED driver
LED_D	X3D12	P1E0	Connects to Serial Data pin on LED driver
LED_OE_N	X3D13	P1F0	Connects to Output Enable on LED driver

Figure 15: User interface GPIO

A green LED (PGOOD) near the USB connector indicates 3V3 and 1V0 supplies are up.

8 Extension Headers

The VocalFusion XVF3500 BaseBoard has two extension headers, J5 and J8, containing digital audio signals, the secondary I2C bus (see §6) and several general purpose GPIOs controlled by the XVF3500.

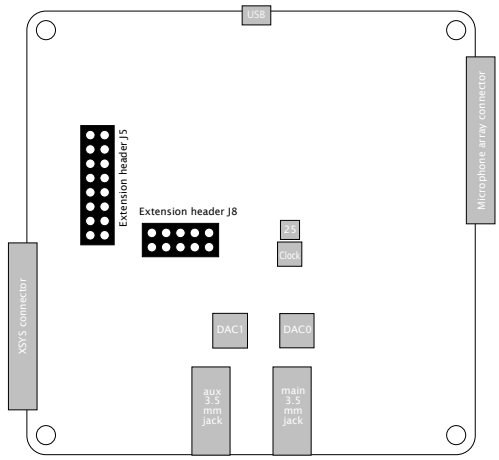

Figure 16: Extension header location

These signals allow the XVF3500 to be connected and controlled by an external applications processor host.

The software image pre-flashed in to the VocalFusion Stereo Dev Kit for Amazon AVS configures the XVF3500 device and the BaseBoard hardware to use these extension headers to connect to an external applications host as defined in §8.1.

The XVF3500 device and BaseBoard hardware *can* support other modes of audio and control connectivity. Examples of these other modes are described in §8.2, and §8.3. To use these modes requires a different XVF3500 software image.

8.1 XVF3500 as the I2S master

- Audio input/output connectivity via I2S signals on J8.

  The XVF3500 is the I2S master.

- Control via I2C on J5.

  The XVF3500 is an I2C slave.

The signal mapping of the extension headers to the XVF3500 GPIO as shown in Figure 17 and Figure 18.

J5 pin	GPIO pin	Port	Signal	Notes
1	X0D13	P1F0		*Not used*
2			GND	Ground
3	X0D12	P1E0		*Not used*
4	X0D11	P1D0		*Not used*
5	X0D00	P1A0		*Not used*
6			GND	Ground
7	X0D39	P1P0		*Not used*
8			GND	Ground
9	X0D38	P1O0	I2C_SDA_EXT	Add a pull-up resistor
10	X0D37	P1N0		*Not used*
11			GND	Ground
12	X0D36	P1M0	I2C_SCL_EXT	Add a pull-up resistor
13			3V3	3.3V from BaseBoard
14			GND	Ground
15			EXT_MCLK	MCLK input (not used)
16			GND	Ground

Figure 17: Extension header J5 GPIO pins (XVF3500 as the I2S master)

J8 pin	GPIO pin	Port	Signal	Notes
1	X2D35	P1L0	I2S_LRCK	I2S LRCLK from XVF3500 to host (and DAC)
2			GND	Ground
3	X2D34	P1K0	I2S_DAC_DATA	I2S data from host to XVF3500 (and DAC)
4			NC	*No connection*
5			GND	Ground
6	X2D36	P1M0	I2S_BCLK	I2S BLCK from XVF3500 to host (and DAC)
7	X2D22	P1H0	MCLK	MCLK output to host (and XVF3500)
8			GND	Ground
9	X2D12	P1E0	X2D12	I2S data from XVF3500 to host
10	X2D11	P1D0	X2D11	*Not used*

Figure 18: Extension header J8 GPIO pins (XVF3500 the I2S master)

8.2 XVF3500 as an I2S slave

To use this mode, remove R67 and insert a 0R link into R17.

- Audio input/output via I2S on J8. The XVF3500 is an I2S slave.
- Control via I2C on J5. The XVF3500 is an I2C slave.
- 24.576 MHz MasterClock generated externally and connected to J5 pin 15.
- Extension headers are mapped to the XVF3500 GPIO as shown in Figure 19 and Figure 20.

8.3 XVF3500 as a USB 2.0 device

If using this mode, both extension headers should be left unconnected.

- Audio input/output via USB. The XVF3500 is a USB Audio Class 1 device.
- Control via USB. The XVF3500 is a custom class control device.

J5 pin	GPIO pin	Port	Signal	Notes
1	X0D13	P1F0		*Not used*
2			GND	Ground
3	X0D12	P1E0		*Not used*
4	X0D11	P1D0		*Not used*
5	X0D00	P1A0		*Not used*
6			GND	Ground
7	X0D39	P1P0		*Not used*
8			GND	Ground
9	X0D38	P1O0	I2C_SDA_EXT	Add a pull-up resistor
10	X0D37	P1N0		*Not used*
11			GND	Ground
12	X0D36	P1M0	I2C_SCL_EXT	Add a pull-up resistor
13			3V3	3.3V from BaseBoard
14			GND	Ground
15			EXT_MCLK	MCLK input from host to XVF3500 (and DAC)
16			GND	Ground

Figure 19: Extension header J5 GPIO pins (XVF3500 an I2S slave)

J8 pin	GPIO pins	Port	Signal	Notes
1	X2D35	P1L0	I2S_LRCK	I2S LRCLK from host to XVF3500 (and DAC)
2			GND	Ground
3	X2D34	P1K0	I2S_DAC_DATA	I2S data from host to DAC
4			NC	*No connection*
5			GND	Ground
6	X2D36	P1M0	I2S_BCLK	I2S BLCK from host to XVF3500 (and DAC)
7	X2D22	P1H0	MCLK	MCLK output (not used)
8			GND	Ground
9	X2D12	P1E0	X2D12	I2S data from XVF3500 to host
10	X2D11	P1D0	X2D11	I2S data from host to XVF3500

Figure 20: Extension header J8 GPIO pins (XVF3500 as an I2S slave)

9 USB Port

The USB micro-B port (J1) provides power for all the on-board circuits and is used to generate the following voltage rails:

- +1V0 (Core voltage to XMOS device)
- +2V5 (for headphone amplifier in DAC device)
- +3V3 for GPIOs and other accessory devices

Voltage tolerance should be as per USB VBUS specification values.

Proper power-on sequence is indicated by power good LED (D1) in bottom side of the board.

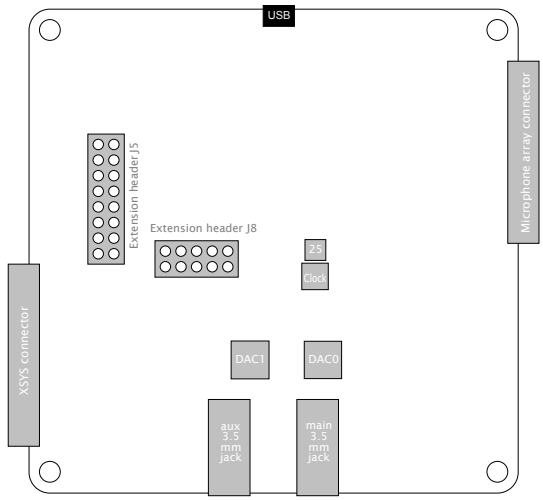

Figure 21: USB components

The data lines from the USB micro-B port (J1) are connected to the XVF3500's integrated USB PHY, and so (with a different XVF3500 software image) *can* be used to provide USB audio and/or control connectivity to the XVF3500 and the BaseBoard.

NOTE:

- the software pre-flashed into the VocalFusion Stereo Dev Kit for Amazon AVS does **not** provide any USB connectivity.
- J1 must be connected at all times to provide power to the VocalFusion XVF3500 BaseBoard, even if the USB interface is not used.

10 Flash Memory

The XVF3500 device needs an external QSPI flash memory, which must be interfaced to the GPIO connections shown in Figure 22.

The flash is located on the bottom of the board, see Figure 23. X2D06 must be pulled high in order to ensure that all tiles are booted from the same flash.

QSPI connection	Pin	Port
QSPI_SS	X0D01	P1B0
QSP_D0	X0D04	P4B0
QSP_D1	X0D05	P4B1
QSP_D2	X0D06	P4B2
QSP_D3	X0D07	P4B3
SPI_CLK	X0D10	P1C0

Figure 22: QSPI Flash GPIO pins

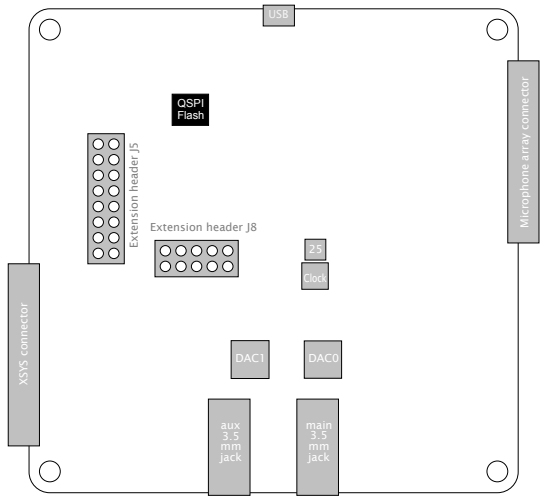

Figure 23: QSPI Flash location

11 xSYS Connector

A standard XMOS xSYS interface (J2) is provided (Figure 24). This can connect to an XMOS xTAG debug adaptor, allowing host debug of the board via JTAG.

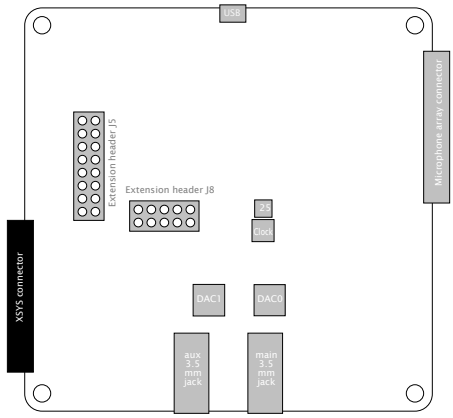

Figure 24: XSYS connector

XSYS signal	xCORE GPIO	Header pin	Description
TMS	See note	7	JTAG Test Mode Select
TCK	See note	9	JTAG Test Clock
TDI	See note	5	JTAG Test Data In - from debug adapter to xCORE
TDO	See note	13	JTAG Test Data Out - from xCORE to debug adapter
RST_N	See note	15	System Reset - active low, resets xCORE device
GND		4, 8, 12, 16, 20	Ground
XL_UP1	X0D43	6	XMOS link, uplink bit 1
XL_UP0	X0D42	10	XMOS link, uplink bit 0
XL_DN0	X0D40	14	XMOS link, downlink bit 0
XL_DN1	X0D41	18	XMOS link, downlink bit 1

Figure 25: xSYS Connector Pinout

Notes:

- JTAG connections occupy dedicated connections

12 VocalFusion XVF3500 BaseBoard Portmap

The tables below detail the port-pin mappings for the VocalFusion XVF3500 BaseBoard, as programmed with USB connectivity software.

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X0D00	$1A^0$					
X0D01	$1B^0$					QSPI_CS
X0D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	QSPI_D0
X0D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	QSPI_D1
X0D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	QSPI_D2
X0D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	QSPI_D3
X0D10	$1C^0$					QSPI_CLK
X0D11	$1D^0$					EXT J5
X0D12	$1E^0$					EXT J5
X0D13	$1F^0$					EXT J5
X0D22	$1G^0$					
X0D23	$1H^0$					
X0D28		$4F^0$	$8C^2$	$16B^2$		BUT_A
X0D29		$4F^1$	$8C^3$	$16B^3$		BUT_B
X0D30		$4F^2$	$8C^4$	$16B^4$		BUT_C
X0D31		$4F^3$	$8C^5$	$16B^5$		BUT_D
X0D32		$4E^2$	$8C^6$	$16B^6$		
X0D33		$4E^3$	$8C^7$	$16B^7$		
X0D36	$1M^0$		$8D^0$	$16B^8$		EXT J5
X0D37	$1N^0$		$8D^1$	$16B^9$		EXT J5
X0D38	$1O^0$		$8D^2$	$16B^{10}$		EXT J5
X0D39	$1P^0$		$8D^3$	$16B^{11}$		EXT J5
X0D40			$8D^4$	$16B^{12}$		XL_DN1
X0D41			$8D^5$	$16B^{13}$		XL_DN0
X0D42			$8D^6$	$16B^{14}$		XL_UP0
X0D43			$8D^7$	$16B^{15}$		XL_UP1
X1D10	$1C^0$					MCLK
X1D11	$1D^0$					
X1D26		$4E^0$	$8C^0$	$16B^0$		

Figure 26: VocalFusion XVF3500 BaseBoard Portmap: Tiles 0 and 1

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X2D00	$1A^0$					
X2D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	Must be pulled high
X2D11	$1D^0$					EXT J8
X2D12	$1E^0$					EXT J8
X2D13	$1F^0$					
X2D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	MIC0_DATA
X2D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	MIC1_DATA
X2D16		$4D^0$	$8B^2$	$16A^{10}$		MIC2_DATA
X2D17		$4D^1$	$8B^3$	$16A^{11}$		MIC3_DATA
X2D18		$4D^2$	$8B^4$	$16A^{12}$		MIC4_DATA
X2D19		$4D^3$	$8B^5$	$16A^{13}$		MIC5_DATA
X2D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	MIC6_DATA
X2D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	MIC7_DATA
X2D22	$1G^0$					MCLK
X2D23	$1H^0$					MIC_CLK
X2D24	$1I^0$					
X2D25	$1J^0$					I2S_DAC1_DATA
X2D28		$4F^0$	$8C^2$	$16B^2$		I2C_SCL
X2D29		$4F^1$	$8C^3$	$16B^3$		I2C_SDA
X2D30		$4F^2$	$8C^4$	$16B^4$		
X2D31		$4F^3$	$8C^5$	$16B^5$		
X2D32		$4E^2$	$8C^6$	$16B^6$		DAC0_RST_N
X2D33		$4E^3$	$8C^7$	$16B^7$		DAC1_RST_N
X2D34	$1K^0$					I2S_DAC0_DATA
X2D35	$1L^0$					I2S_LRCK
X2D36	$1M^0$		$8D^0$	$16B^8$		I2S_BCLK
X3D00	$1A^0$					LED_STCP
X3D01	$1B^0$					LED_SHCP
X3D12	$1E^0$					LED_D
X3D13	$1F^0$					LED_OE_N

Figure 27: xCORE-VocalFusion Evaluation Board Portmap: Tiles 2 and 3

13 Raspberry Pi Interface Cable

The VocalFusion Stereo Dev Kit for Amazon AVS is supplied with a cable to interface to the VocalFusion XVF3500 BaseBoard (via J5 and J8, see §8) to a Raspberry Pi.

The interface cable makes the connections as shown in the table below.

Raspberry Pi		cable	BaseBoard			XVF3500		Notes
Signal	J8	color	J5	J8	Signal	Pin	Port	
SDA	3	white	9		I2C_SDA_EXT	X0D38	P1O0	I2C SDA between Pi (master) and XVF3500 (slave)
SCL	5	white	12		I2C_SCL_EXT	X0D36	P1M0	I2C SCL between Pi (master) and XVF3500 (slave)
GND	6	black		2	GND			Ground
GND	9	black		5	GND			Ground
I2S_BCLK	12	white		6	I2S_BCLK	X2D36	P1M0	I2S BLCK from XVF3500 to Pi
GND	14	black		8	GND			Ground
SPI_MOSI	19	white	7		X0D39	X0D39	P1P0	*not used*
GND	20	black	2		GND			Ground
SPI_MISO	21	white	5		X0D00	X0D00	P1A0	*not used*
SPI_SCLK	23	red	1		X0D13	X0D13	P1F0	*not used*
SPI_CE0	24	white	3		X0D12	X0D12	P1E0	*not used*
GND	25	black	6		GND			Ground
GND	30	black	8		GND			Ground
GND	34	black	11		GND			Ground
I2S_LRCLK	35	red		1	I2S_LRCK	X2D35	P1L0	I2S LRCLK from XVF3500 to Pi
I2S_DIN	38	white		9	X2D12	X2D12	P1E0	I2S data from XVF3500 to Pi
GND	39	black	14		GND			Ground
I2S_DOUT	40	white		3	I2S_DAC_DATA	X2D34	P1K0	I2S data from Pi to XVF3500 and DAC

Figure 28: Raspberry Pi interface cable

For more details on how to connect and setup a Raspberry Pi, see:

- http://www.xmos.com/vocalfusion-stereoavs

14 Operating Requirements

A USB 2.0 high-speed compliant cable, of less than 3m in length, should be used when operating the VocalFusion Stereo Dev Kit for Amazon AVS.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the VocalFusion Stereo Dev Kit for Amazon AVS with appropriate ESD precautions in place.

15 Dimensions

The VocalFusion XVF3500 BaseBoard is 90x90mm square and board thickness of 1.6mm.

16 RoHS and REACH

The VocalFusion Stereo Dev Kit for Amazon AVS complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The VocalFusion Stereo Dev Kit for Amazon AVS is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU.

17 Schematics

The schematics for the VocalFusion XVF3500 BaseBoard included in the kit, are shown in the first five figures below, followed by the schematics for the linear microphone array board.

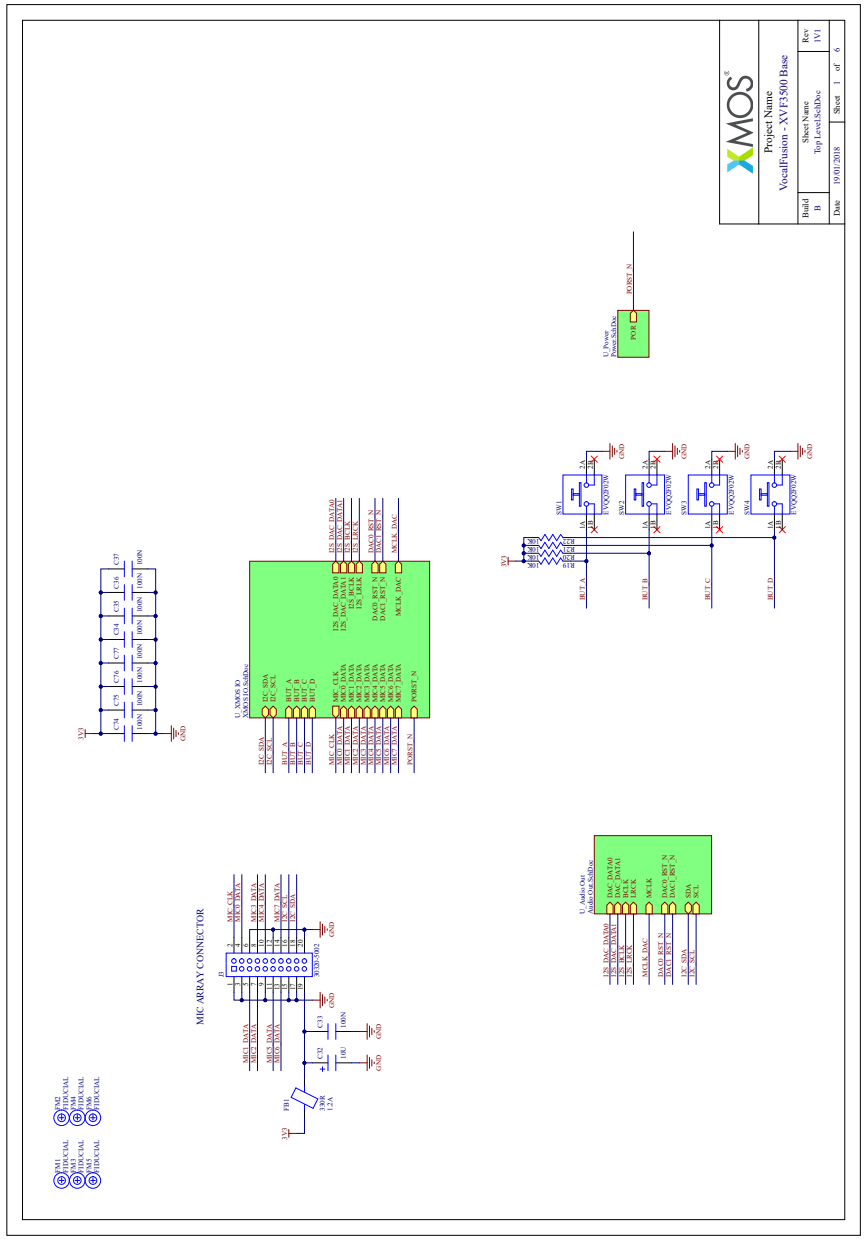

Figure 29: VocalFusion XVF3500 BaseBoard - XVF3500 configuration

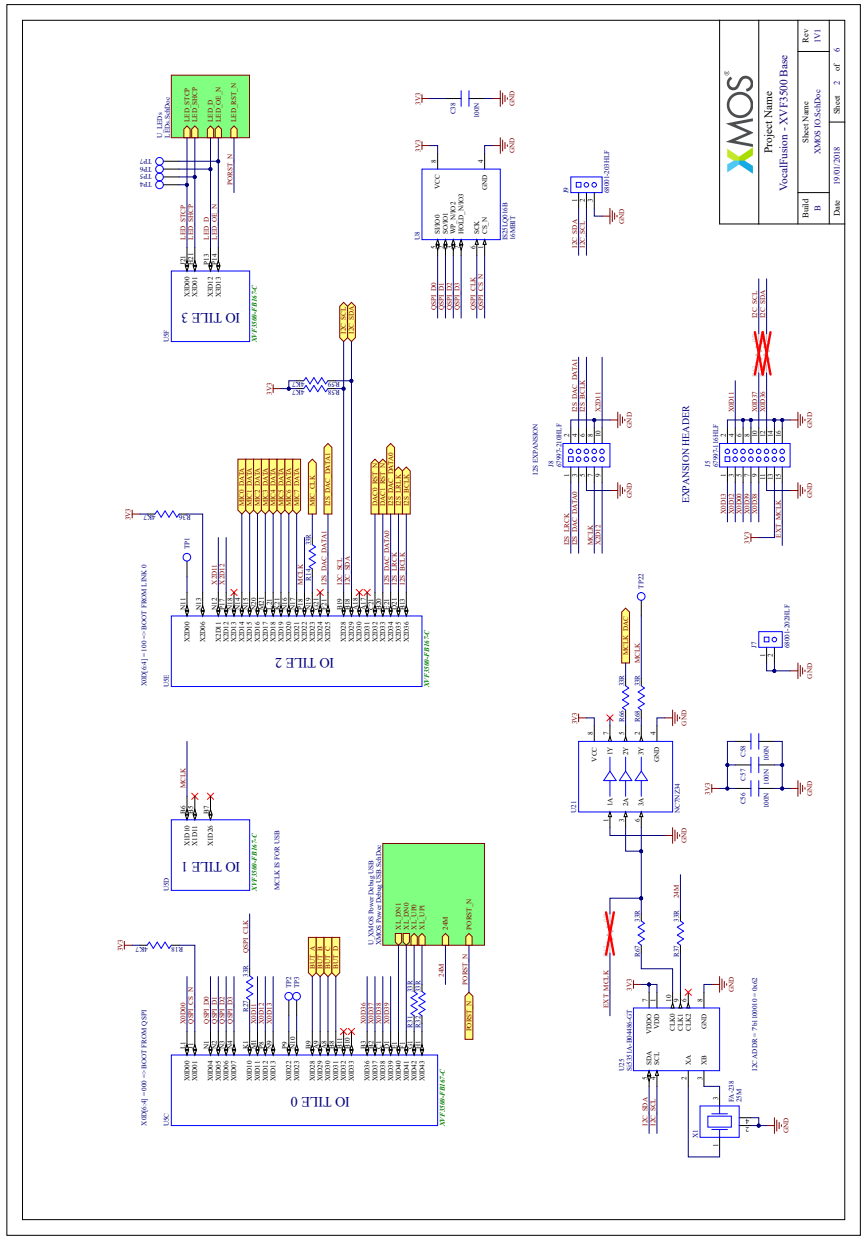

Figure 30: VocalFusion XVF3500 BaseBoard - extension header, buttons, Microphone header, Tile 0 IO

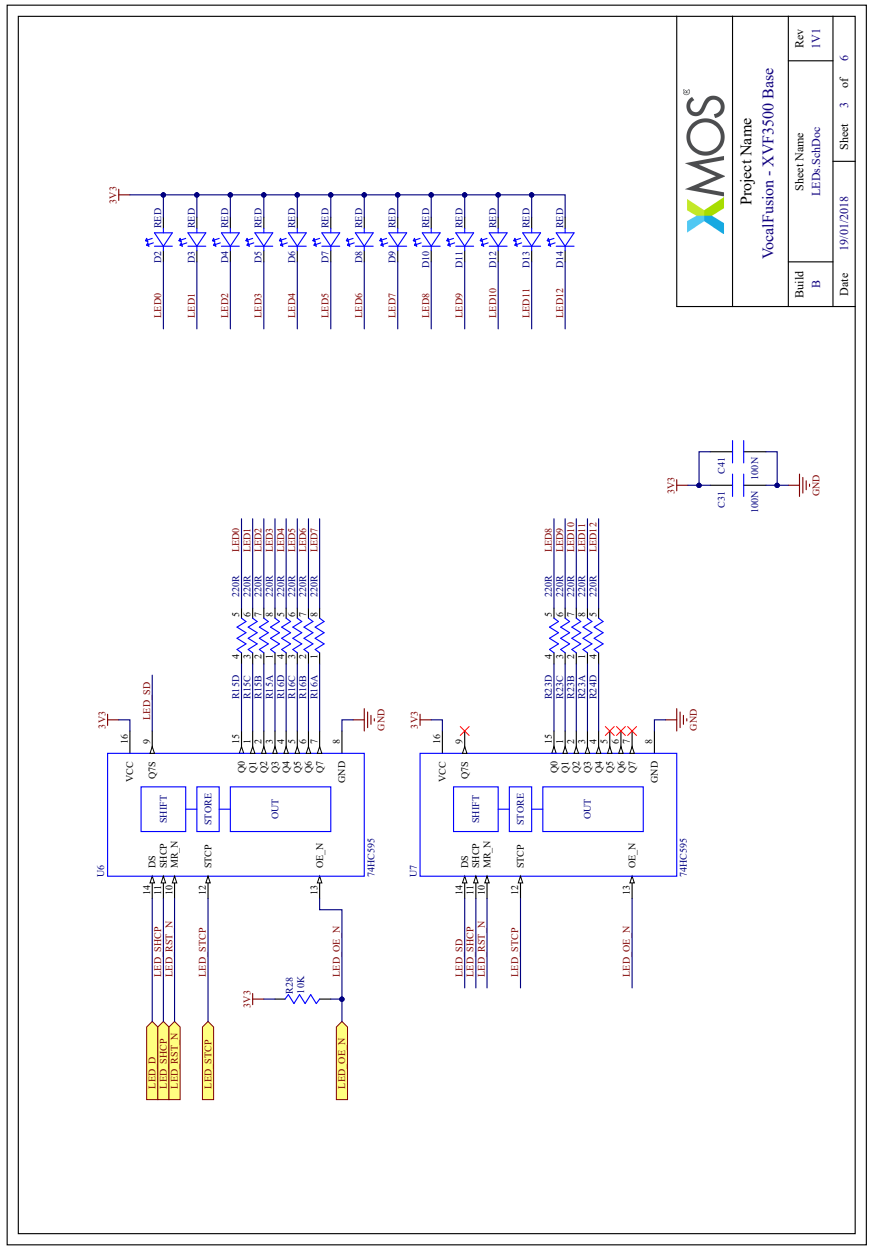

Figure 31: VocalFusion XVF3500 BaseBoard - LEDs

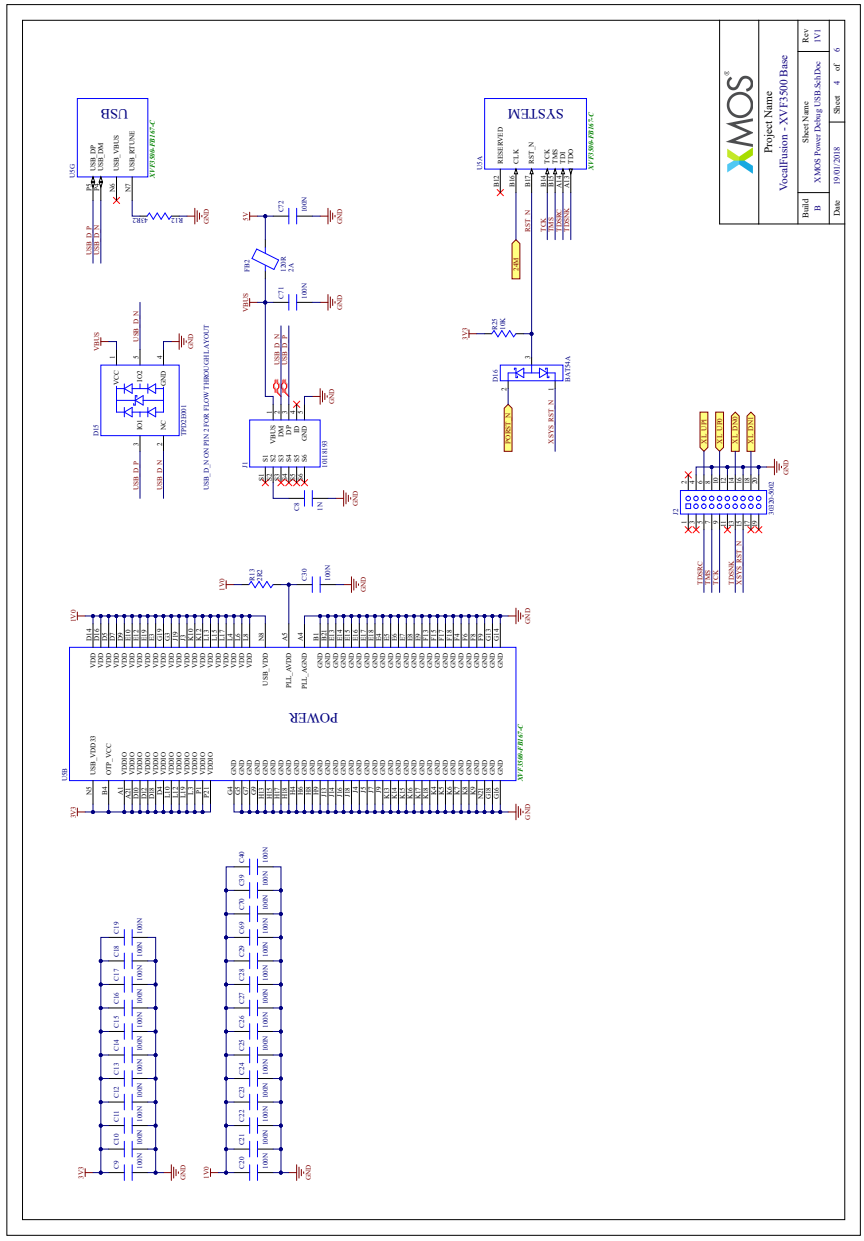

Figure 32: VocalFusion XVF3500 BaseBoard - USB, XVF3500 power and ground

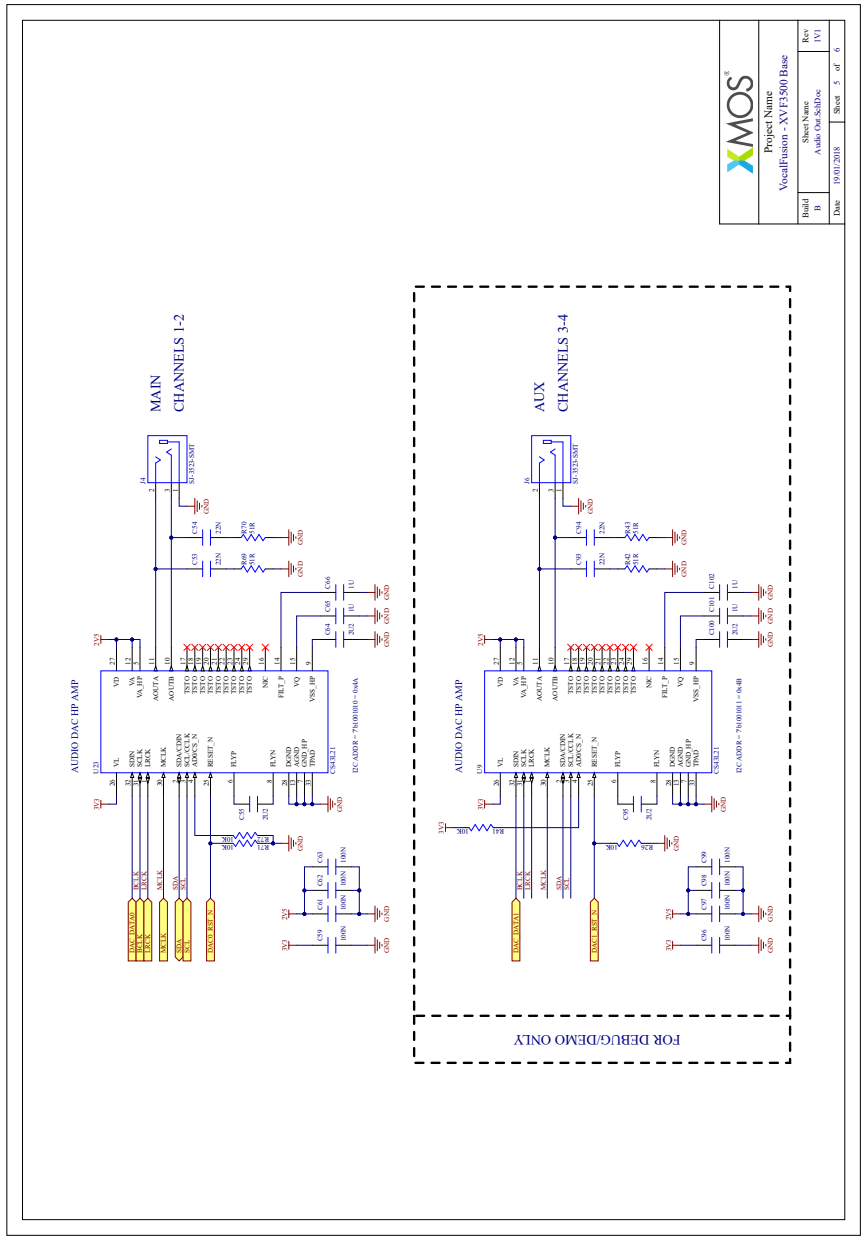

Figure 33: VocalFusion XVF3500 BaseBoard -Dual stereo DAC

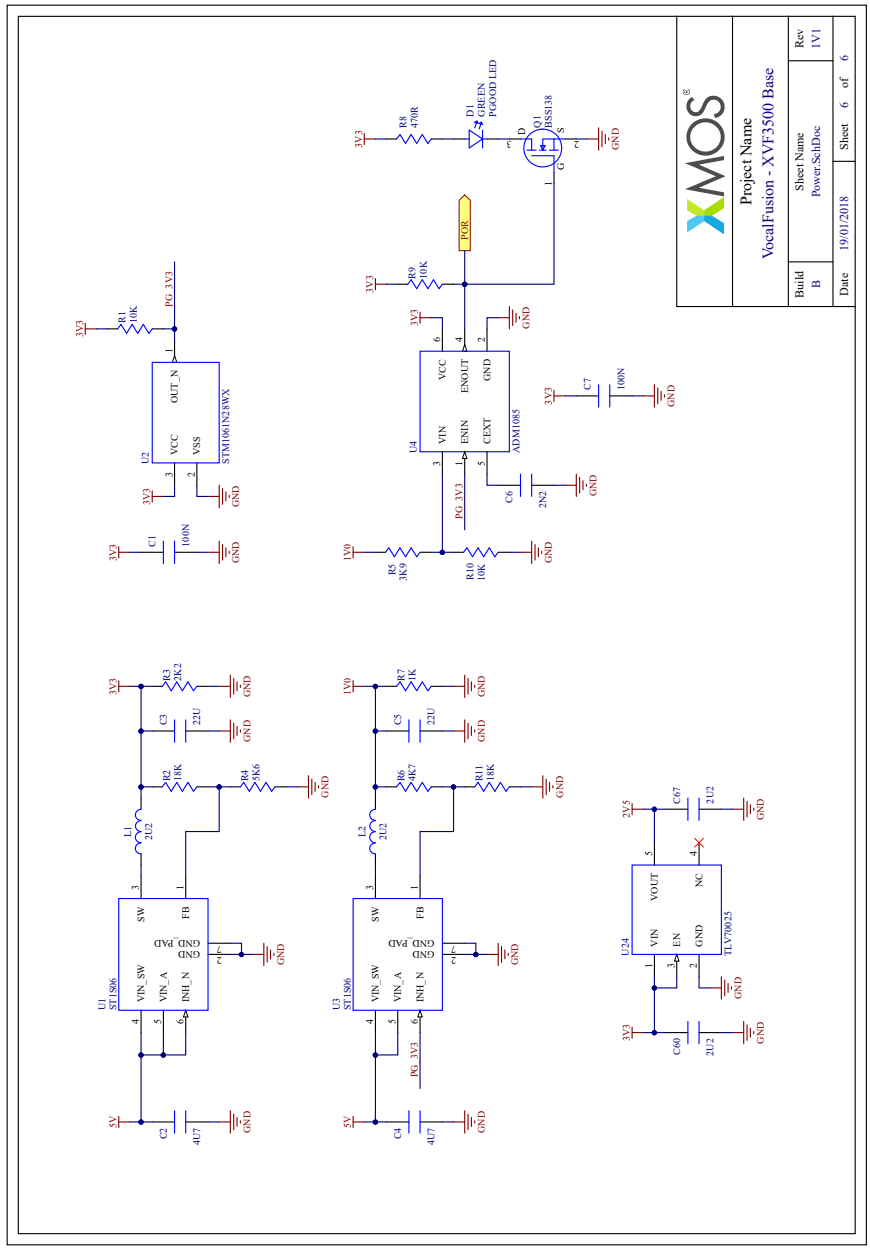

Figure 34: VocalFusion XVF3500 BaseBoard - voltage rail LDOs and reset circuit

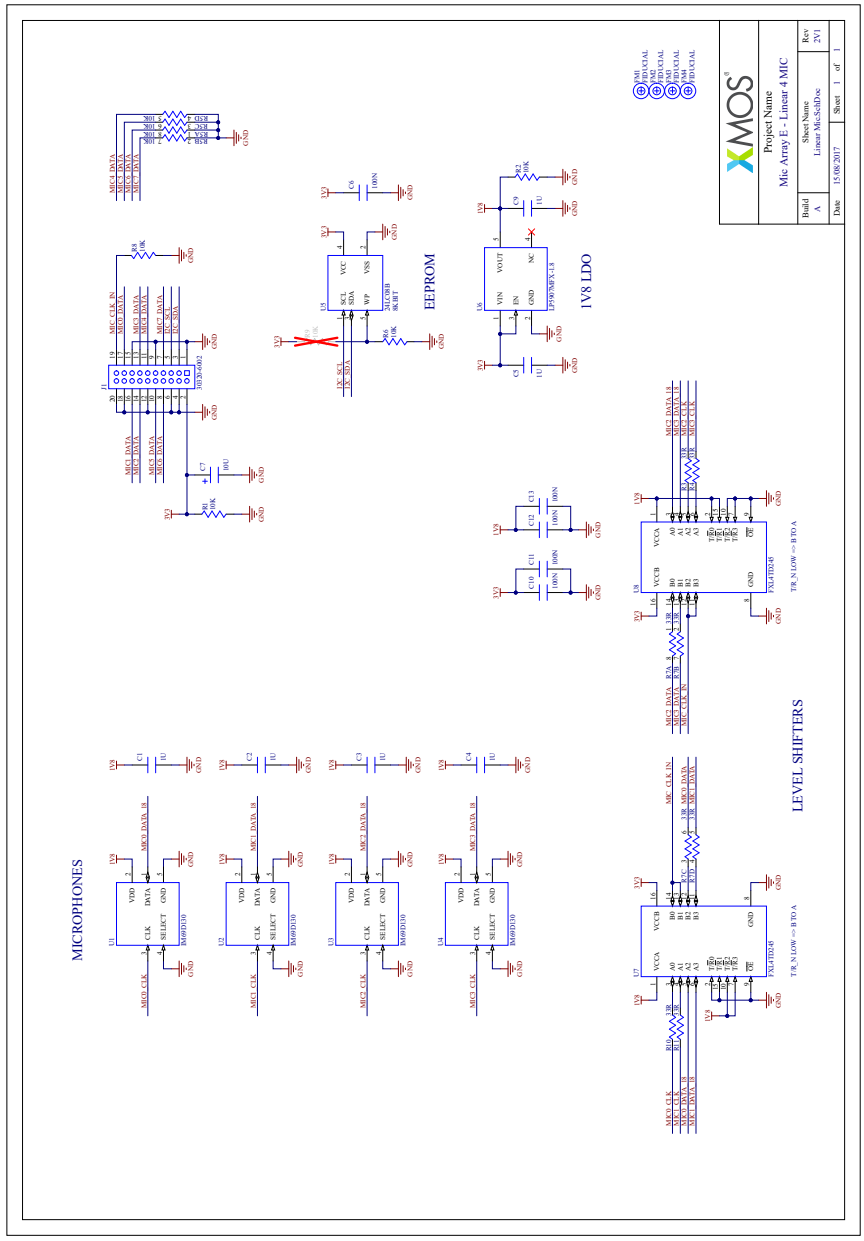

Figure 35: xCORE VocalFusion Linear Microphone Board