User Guide for

FEBFSL4110LR_CS01U06A

Integrated Controller

FSL4110LR

6.0 W Auxiliary Power Supply

Featured Fairchild Product:

FSL4110LR

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Table of Contents

This user guide supports the evaluation kit for the FSL4110LR. It should be used in conjunction with the FSL4110LR datasheet as well as Fairchild's application notes and technical support team. Please visit Fairchild's website at www.fairchildsemi.com.

1. Introduction

This document is an engineering report describing measured performance of the FSL4110LR. The input voltage range is 85 V_{RMS} – 460 V_{RMS}, there is one DC output of 300 mA at 20V $_{MAX}$. This document contains a general description of FSL4110LR, the power supply specification, schematic, bill of materials, and the typical operating characteristics.

1.1. General Description

The FSL4110LR is an integrated Pulse Width Modulation (PWM) controller and 1000 V avalanche rugged SenseFET specifically designed for high input voltage offline Switching Mode Power Supplies (SMPS) with minimal external components. VCC can be supplied through integrated high-voltage power regulator without auxiliary bias winding.

The integrated PWM controller includes a fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, soft-start, temperature-compensated precise current sources for loop-compensation, and variable protection circuitry.

Compared with a discrete MOSFET and PWM controller solution, the FSL4110LR reduces total cost, component count, PCB size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost-effective design of a flyback converter.

1.2. Features

- Built-in Avalanche Rugged 1000 V SenseFET
- Precise Fixed Operating Frequency: 50 kHz
- VCC can be supplied from either bias-winding or self-biasing.
- Soft Burst-Mode Operation Minimizing Audible Noise
- Random Frequency Fluctuation for Low EMI
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis. Under-Voltage Lockout (UVLO) and Line Over-Voltage Protection (LOVP) with Hysteresis.
- Built-in Internal Startup and Soft-Start Circuit
- Fixed 1.6 s Restart Time for Safe Auto-Restart Mode of All Protections

1.3. Internal Block Diagram

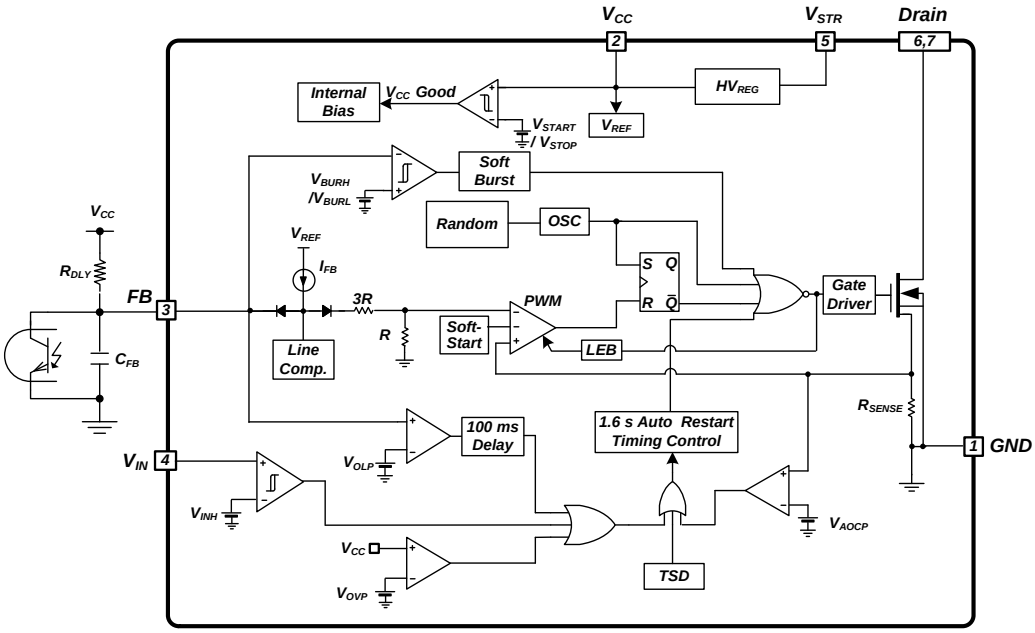

Figure 1. Block Diagram

2. Specification for Evaluation Board

Table 1. Evaluation Board Specifications

Main Controller		FSL4110LRN
Input	**Frequency Range**	60 Hz
	Voltage Range	85 V_{AC} ~ 460 V_{AC}
Output	**Power**	< 6 W
	Voltage	< 20 V
	Current	Typ. 0.3 A
Board Dimensions	143 mm x 40 mm	

All data of the evaluation board were measured under a condition where the board was enclosed in a case and external temperature was around 25°C.

3. Photographs

To measure drain current, change from jumper to wire.
But keep the jumper in the other cases.

Figure 2. Top View

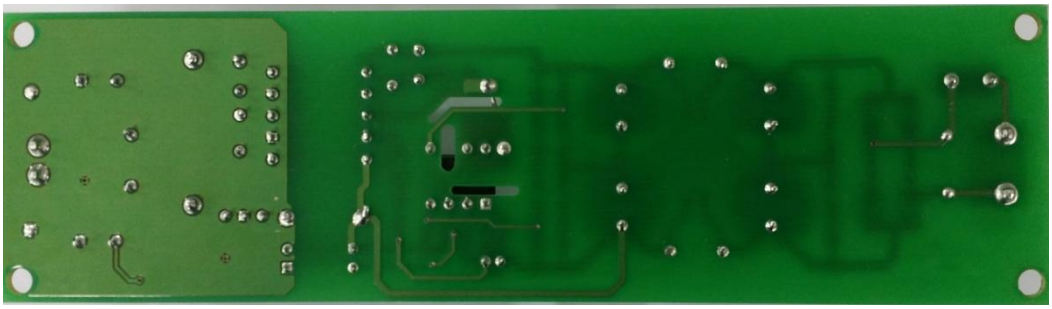

Figure 3. Bottom View

4. Printed Circuit Board

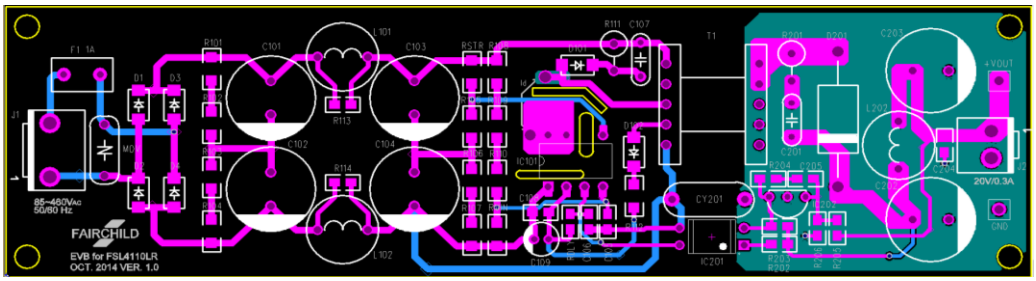

Figure 4. Board Layout

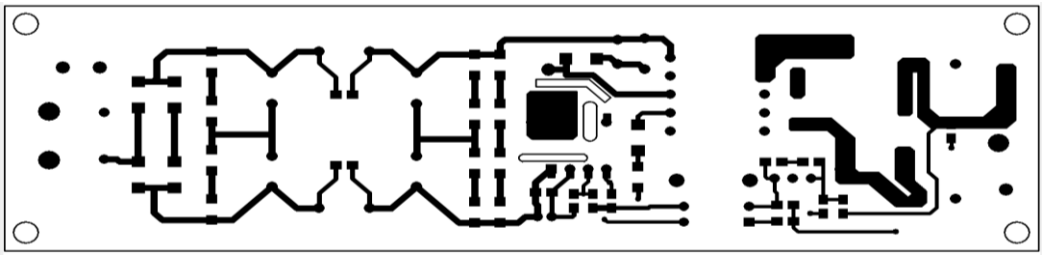

Figure 5. Printed PCB, Top Side

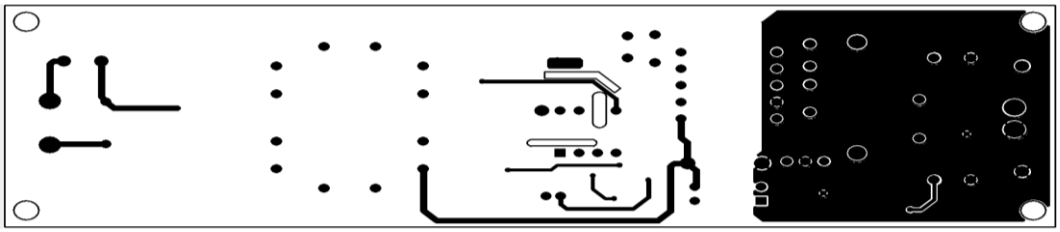

Figure 6. Printed PCB, Bottom Side

5. Schematic

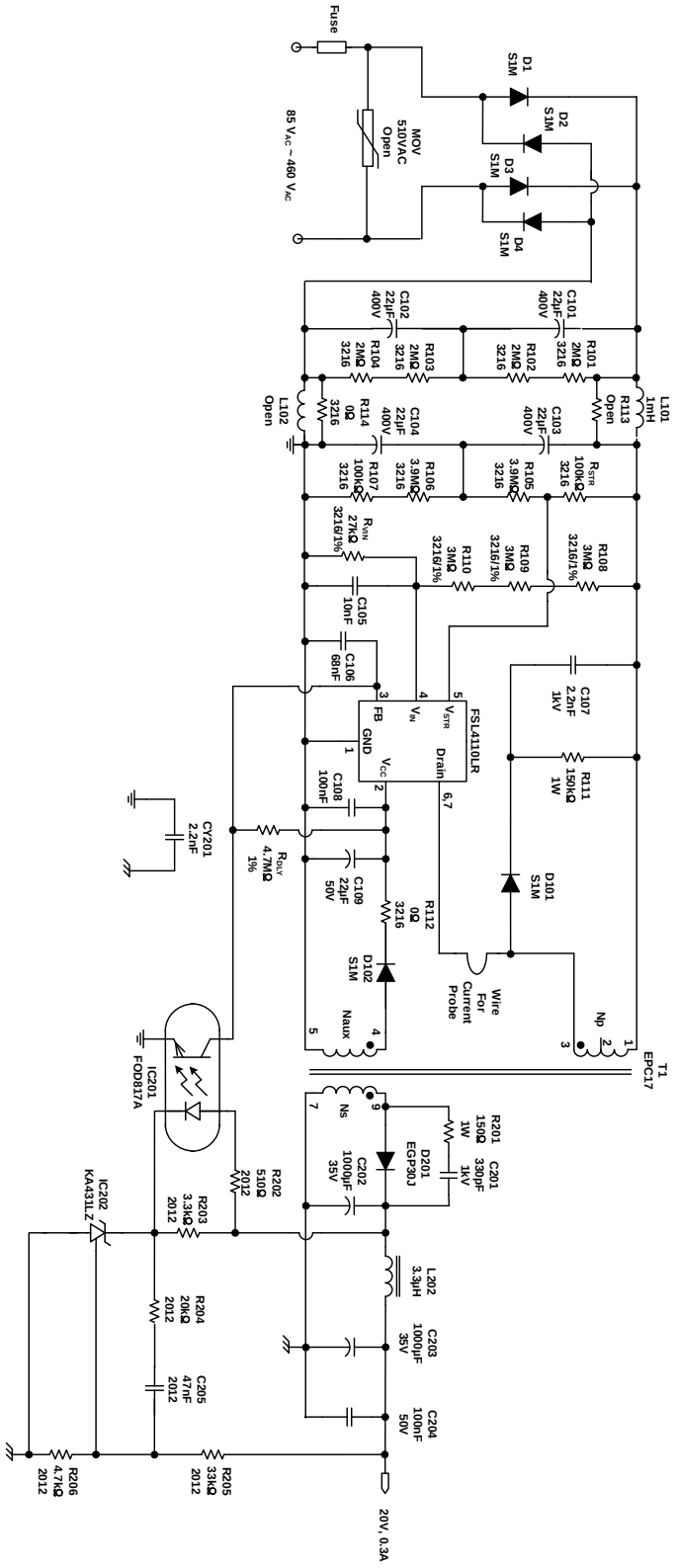

Figure 7. Evaluation Board Schematic

6. Bill of Materials

Item No.	Part Reference	Part Number	Qty.	Description
1	IC101	FSL4110LRN	1	7-DIP, Fairchild Semiconductor
2	IC201	FOD817A	1	4-DIP, Fairchild Semiconductor
3	IC202	KA431LZ	1	TO-92, Fairchild Semiconductor
4	D1, D2, D3, D4, D101, D102	S1M	6	1000 V / 1 A General Purpose Rectifiers, SMA, Fairchild Semiconductor
5	D202	EGP30J	1	1000 V / 3 A Rectifiers, DO-201AD, Fairchild Semiconductor
6	F1	SS-5-1A	1	1 A Fuse
7	MOV	Open		Open
8	L101	1 mH	1	Filter Inductor, 10Φ
9	L102	Open		Open
10	L202	3.3 µH	1	Filter Inductor, 8Φ
11	T1	Lm = 1.4 mH	1	EPC17 Core
12	R101, R102, R103, R104	2 MΩ	4	SMD Resistor 3216
13	RSTR, R107	100 kΩ	2	SMD Resistor 3216
14	R105, R106	3.9 MΩ	2	SMD Resistor 3216
15	R108, R109, R110	3 MΩ	3	SMD Resistor 3216
16	RVIN	27 kΩ	1	SMD Resistor 3216 / 1%
17	R111	150 kΩ	1	Resistor 1 W
18	R112, R114	0 Ω	2	SMD Resistor 3216
19	R113	Open		Open
20	RDLY	4.7 MΩ	1	SMD Resistor 2012 / 1%
21	R201	150 Ω	1	Resistor 1 W
22	R202	510 Ω	1	SMD Resistor 2012
23	R203	3.3 kΩ	1	SMD Resistor 2012
24	R204	20 kΩ	1	SMD Resistor 2012
25	R205	33 kΩ	1	SMD Resistor 2012 / 1%
26	R206	4.7 kΩ	1	SMD Resistor 2012 / 1%
27	C101, C102, C103, C104	22 µF / 400 V	4	Electrolytic Capacitor, 105°C
28	C105	10 nF / 50 V	1	SMD Capacitor 2012
29	C106	68 nF / 50 V	1	SMD Capacitor 2012
30	C107	2.2 nF / 1 kV	1	Ceramic Capacitor
31	C108	100 nF / 50 V	1	SMD Capacitor 2012
32	C109	22 µF / 50 V	1	Electrolytic Capacitor, 105°C
33	C201	330 pF / 1 kV	1	Ceramic Capacitor
34	C202, C203	1000 µF / 35 V	2	Ultra-Low Impedance Electrolytic Capacitor, 105°C
35	C204	100 nF / 50 V	1	SMD Capacitor 2012
36	C205	47 nF / 50 V	1	SMD Capacitor 2012
37	CY201	2.2 nF	1	Y-Capacitor

7. Transformer Design

- Core: EPC17 (PC-40)
- Bobbin: 10 Pins

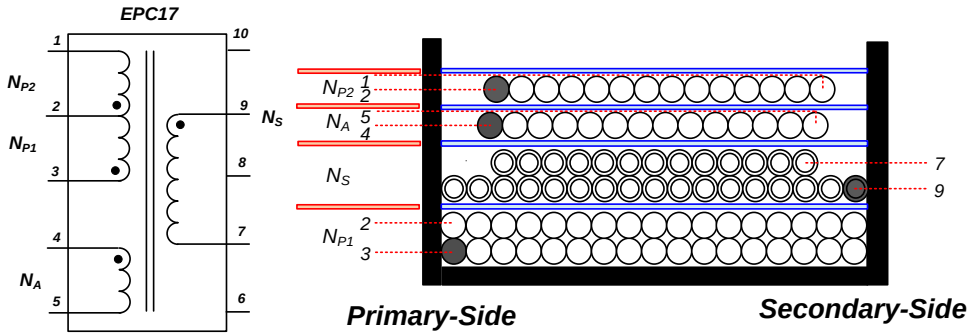

Figure 8. Transformer Specifications & Construction

Table 2. Winding Specifications

No.	Winding	Pin (S → F)	Wire	Turns	Winding Method
1	N_{P1}	3 → 2	0.20 Φ * 1	72 Ts	Solenoid Winding
2	Insulation: Polyester Tape t = 0.05 mm, 3-Layer				
3	N_S	9 → 7	0.20 Φ (TEX) * 1	27 Ts	Solenoid Winding
4	Insulation: Polyester Tape t = 0.05 mm, 3-Layer				
5	N_A	4 → 5	0.15 Φ * 1	20 Ts	Solenoid Winding
6	Insulation: Polyester Tape t = 0.05 mm, 3-Layer				
7	N_{P2}	2 → 1	0.20 Φ * 1	33 Ts	Center Solenoid Winding
8	Outer Insulation: Polyester Tape t = 0.05 mm, 3-Layer				

Table 3. Electrical Characteristics

	Pin	Specification	Remark
Inductance	1 - 3	1.4 mH ±7%	1 kHz, 1 V
Leakage	1 - 3	Max. 20 µH	Short All Output Pins

8. Test Conditions

Table 4. Test Conditions & Test Equipment

Evaluation Board #	FEBFSL4110LR_CS01U06A
Test Date	November 04, 2014
Test Equipment	AC Source: 6800 Series by EXTECH Electronic Load: EML-05B by FUJITSU Oscilloscope: WaveRunner 104Xi-A by LeCroy Power Meter: PZ4000 by YOKOGAWA Multi Meter: 45 by FLUKE
Test Items	1. Startup Performance 2. Normal Operation 3. Voltage Stress of Drain and Secondary Diode 4. Output Ripple and Noise 5. Load Transient 6. Output Line & Load Regulation 7. Hold-Up Time 8. Output Short Test 9. Abnormal Over Current Test 10. Efficiency 11. Operating Temperature 12. Electromagnetic Interference (EMI)

9. Performance of Evaluation Board

9.1. Startup Performance

Test Condition: Measure the time interval between AC plug-in and stable output.

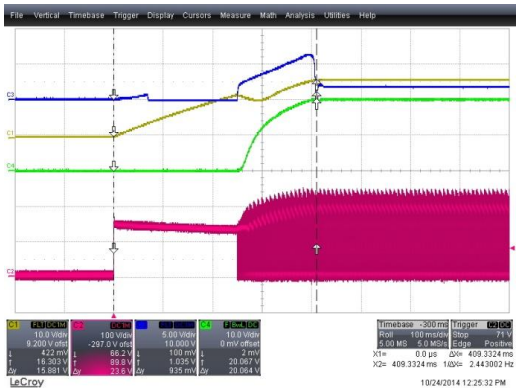

Figure 9. Startup Time = 409 ms, 85 V_{AC}, Full-Load Condition (CH1: V_{CC} (10 V/div), CH2: V_{DS} (100 V/div), CH3: V_{FB} (5 V/div), CH4: V_{OUT} (10 V/div), Time: 100 ms/div)

Figure 10. Startup Time = 293 ms, 460 V_{AC}, Full-Load Condition (CH1: V_{CC} (10 V/div), CH2: V_{DS} (200 V/div), CH3: V_{FB} (5 V/div), CH4: V_{OUT} (10 V/div), Time: 100 ms/div)

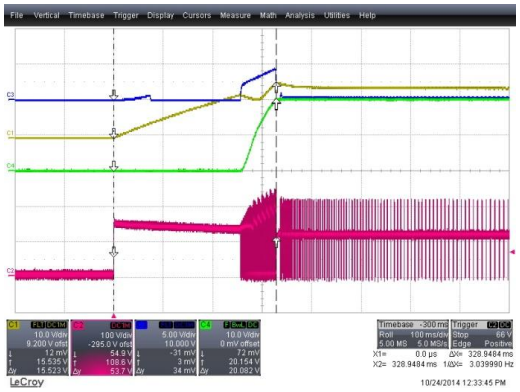

Figure 11. Startup Time = 329 ms, 85 V_{AC}, No-Load Condition (CH1: V_{CC} (10 V/div), CH2: V_{DS} (100 V/div), CH3: V_{FB} (5 V/div), CH4: V_{OUT} (10 V/div), Time: 100 ms/div)

Figure 12. Startup Time = 216 ms, 460 V_{AC}, Full-Load Condition (CH1: V_{CC} (10 V/div), CH2: V_{DS} (200 V/div), CH3: V_{FB} (5 V/div), CH4: V_{OUT} (10 V/div), Time: 100 ms/div)

9.2. Normal Operation

Test Condition: Measure normal operation.

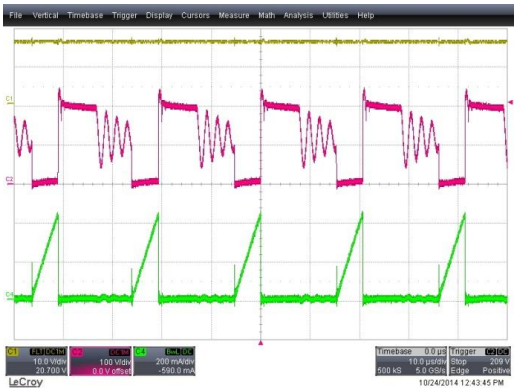

Figure 13. 85 V_{AC}, Full-Load Condition (CH1: V_{CC} (10 V/div), CH2: V_{DS} (100 V/div), CH4: I_{DS} (200 mA/div), Time: 10 µs/div)

Figure 14. 460 V_{AC}, Full-Load Condition (CH1: V_{CC} (10 V/div), CH2: V_{DS} (500 V/div), CH4: I_{DS} (500 mA/div), Time: 10 µs/div)

Figure 15. 85 V_{AC}, No-Load Condition (CH1: V_{CC} (10 V/div), CH2: V_{DS} (100 V/div), CH4: I_{DS} (200 mA/div), Time: 5 ms/div)

Figure 16. 460 V_{AC}, No-Load Condition (CH1: V_{CC} (10 V/div), CH2: V_{DS} (500 V/div), CH4: I_{DS} (500 mA/div), Time: 20 ms/div)

9.3. Voltage Stress of Drain and Secondary Diode

Test Condition: Measure the voltage stress on the FSL4110LR and secondary diode.

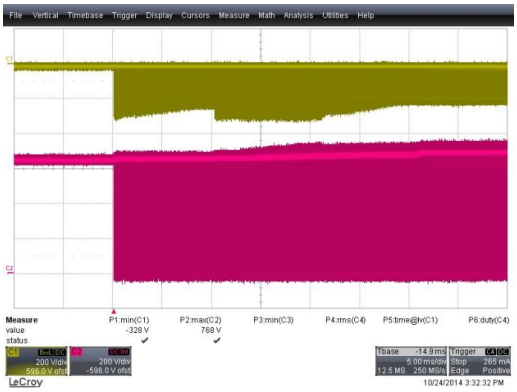

Figure 17. V_{DS}=768 V, V_{DIODE}=328 V, Startup, Full-Load Condition, 460 V_{AC}, (CH1: V_{DIODE} (200 V/div), CH2: V_{DS} (200 V/div), Time: 5 ms/div)

Figure 18. V_{DS}=786 V, V_{DIODE}=249 V, Steady-State, Full-Load Condition, 460 V_{AC}, (CH1: V_{DIODE} (200 V/div), CH2: V_{DS} (200 V/div), Time: 5 µs/div)

Figure 19. V_{DS}=731 V, V_{DIODE}=328 V, Output Short, Full-Load Condition, 460 V_{AC}, (CH1: V_{DIODE} (200 V/div), CH2: V_{DS} (200 V/div), Time: 50 ms/div)

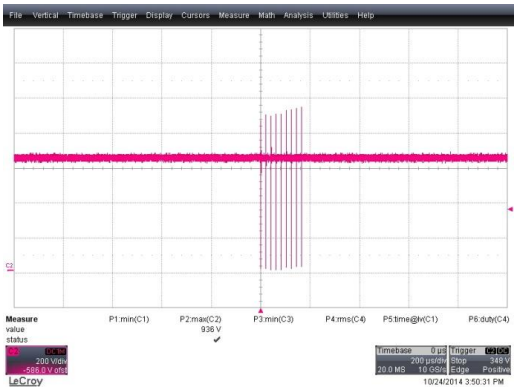

Figure 20. V_{DS}=936 V, Secondary Diode Short (AOCP), Full-Load Condition, 460 V_{AC}, (CH1: V_{DIODE} (200 V/div), CH2: V_{DS} (200 V/div), Time: 200 µs/div)

9.4. Output Ripple and Noise

Test Condition: Ripple and noise are measured by using 20 MHz bandwidth limited oscilloscope with a 10 µF / 50 V capacitor paralleled with a high-frequency 0.1 µF capacitor across a output as Figure 21.

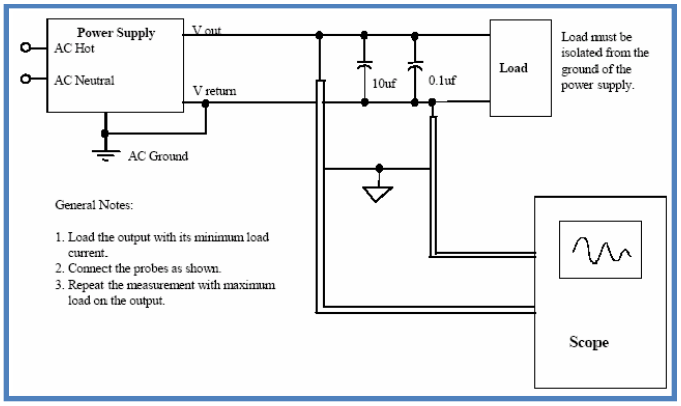

Figure 21. Recommended Test Setup

Table 5. Test Result

	No-Load	25% Load	50% Load	75% Load	Full-Load
85 V_{AC}	22.4 mVp-p	20.5 mVp-p	27.5 mVp-p	35.8 mVp-p	37.8 mVp-p
110 V_{AC}	23.7 mVp-p	20.5 mVp-p	28.2 mVp-p	35.2 mVp-p	38.4 mVp-p
230 V_{AC}	42.2 mVp-p	27.5 mVp-p	31.4 mVp-p	36.5 mVp-p	39 mVp-p
265 V_{AC}	43.5 mVp-p	30.1 mVp-p	32.6 mVp-p	37.1 mVp-p	39.7 mVp-p
350 V_{AC}	46.1 mVp-p	35.2 mVp-p	36.5 mVp-p	39 mVp-p	41.6 mVp-p
400 V_{AC}	55.7 mVp-p	39 mVp-p	39.4 mVp-p	41 mVp-p	43.5 mVp-p
460 V_{AC}	62.7 mVp-p	44.8 mVp-p	42.9 mVp-p	42.2 mV-p	44.2 mVp-p

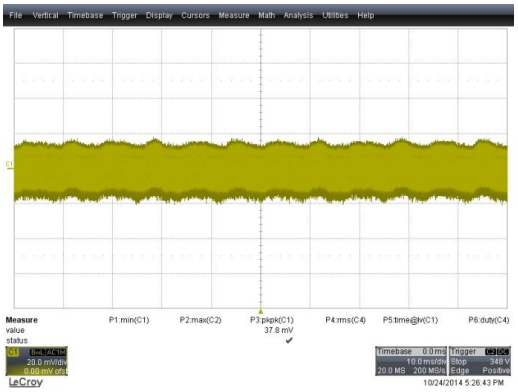

Figure 22. V_{OUT_RIPPLE} = 37.8 mVp-p, Output with 85 V_{AC} and Full-Load Condition, (CH1: V_{OUT} (20 mV_{AC}/div), Time: 10 ms/div)

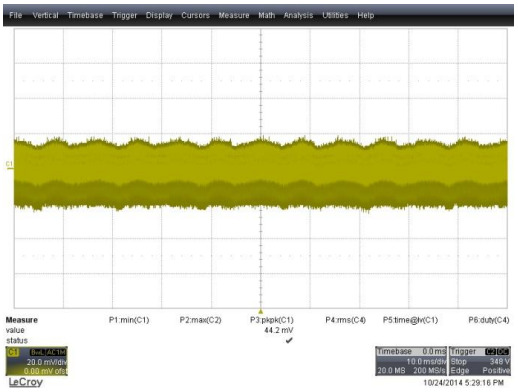

Figure 23. V_{OUT_RIPPLE} = 44.2 mVp-p, Output with 460 V_{AC} and Full-Load Condition, (CH1: V_{OUT} (20 mV_{AC}/div), Time: 10 ms/div)

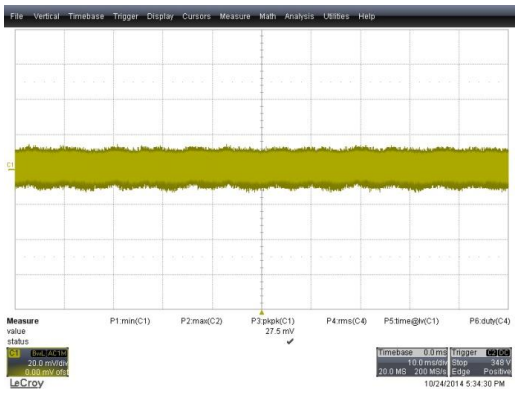

Figure 24. V_{OUT_RIPPLE} = 27.5 mVp-p, Output with 85 V_{AC} and 50% Load Condition, (CH1: V_{OUT} (20 mV_{AC}/div), Time: 10 ms/div)

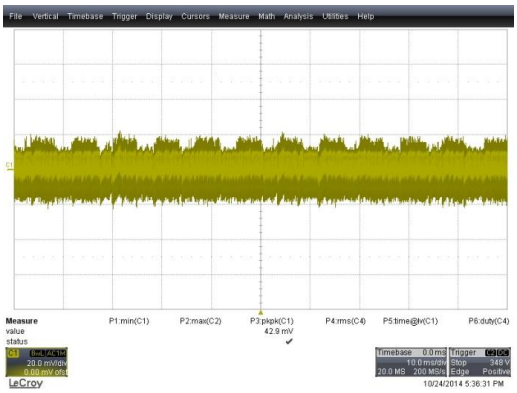

Figure 25. V_{OUT_RIPPLE} = 42.9 mVp-p, Output with 460 V_{AC} and 50% Load Condition, (CH1: V_{OUT} (20 mV_{AC}/div), Time: 10 ms/div)

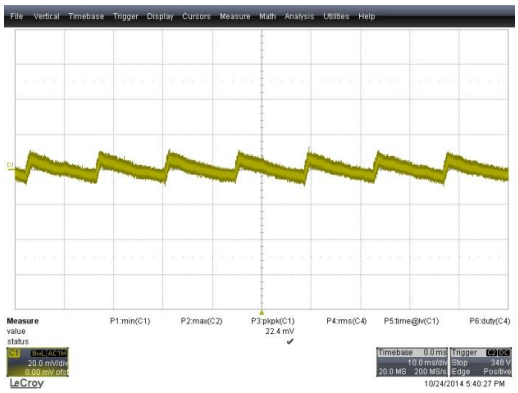

Figure 26. V_{OUT_RIPPLE} = 22.4 mVp-p, Output with 85 V_{AC} and No-Load Condition, (CH1: V_{OUT} (20 mV_{AC}/div), Time: 10 ms/div)

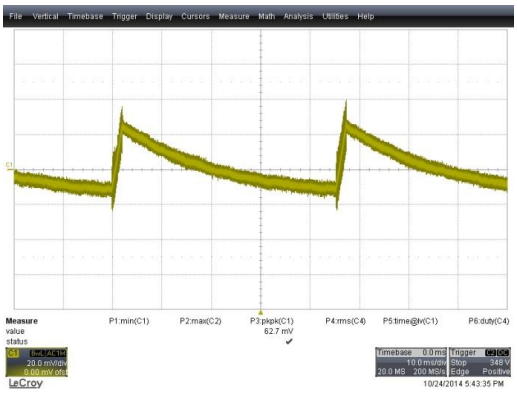

Figure 27. V_{OUT_RIPPLE} = 62.7 mVp-p, Output with 460 V_{AC} and No-Load Condition, (CH1: V_{OUT} (20 mV_{AC}/div), Time: 10 ms/div)

9.5. Load Transient

Test Condition: Load Transient is measured by using 20 MHz bandwidth limited oscilloscope with a 10 µF / 50 V capacitor paralleled with a high-frequency 0.1 µF capacitor across a output as Figure 21.

Table 6. Test Result

		85 V_{AC}	110 V_{AC}	230 V_{AC}	265 V_{AC}	350 V_{AC}	400 V_{AC}	460 V_{AC}
Full-Load → No-Load	Overshoot	143 mV	146 mV	143 mV	150 mV	140 mV	147 mV	140 mV
	Undershoot	57 mV	59 mV	59 mV	57 mV	57 mV	56 mV	54 mV
	Peak-Peak	200 mV	205 mV	202 mV	207 mV	197 mV	203 mV	194 mV
No-Load → Full-Load	Overshoot	79 mV	78 mV	72 mV	72 mV	69 mV	67 mV	75 mV
	Undershoot	271 mV	284 mV	269 mV	283 mV	253 mV	268 mV	250 mV
	Peak-Peak	350 mV	362 mV	341 mV	355 mV	322 mV	335 mV	325 mV

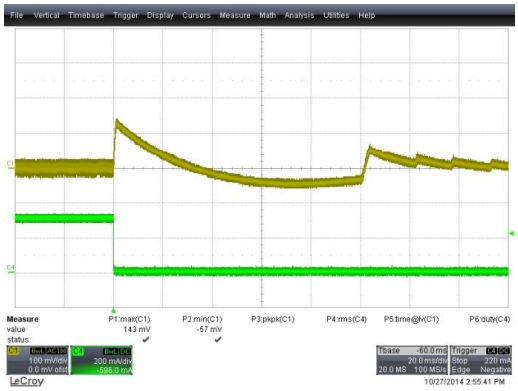

Figure 28. V_{OUT_RIPPLE} = 200 mVp-p, Output with 85 V_{AC}, Full-Load → No-Load (CH1: V_{OUT} (100 mV_{AC}/div), CH4: I_{OUT} (200 mA/div), Time: 20 ms/div)

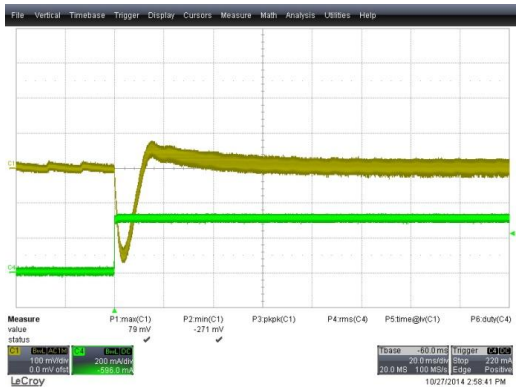

Figure 29. V_{OUT_RIPPLE} = 350 mVp-p, Output with 85 V_{AC}, No-Load → Full-Load (CH1: V_{OUT} (100 mV_{AC}/div), CH4: I_{OUT} (200 mA/div), Time: 20 ms/div)

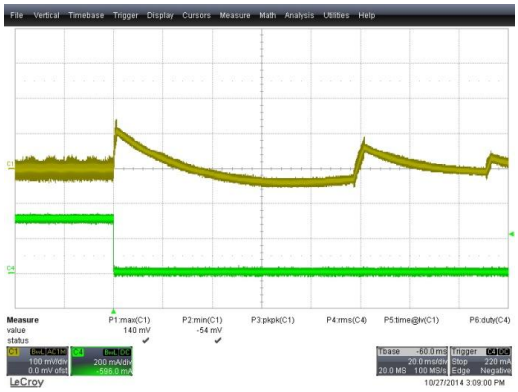

Figure 30. V_{OUT_RIPPLE} = 194 mVp-p, Output with 460 V_{AC}, Full-Load → No-Load (CH1: V_{OUT} (100 mV_{AC}/div), CH4: I_{OUT} (200 mA/div), Time: 20 ms/div)

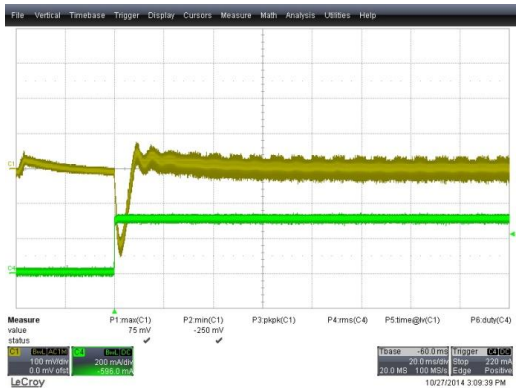

Figure 31. V_{OUT_RIPPLE} = 325 mVp-p, Output with 460 V_{AC}, No-Load → Full-Load (CH1: V_{OUT} (100 mV_{AC}/div), CH4: I_{OUT} (200 mA/div), Time: 20 ms/div)

9.6. Output Line and Load Regulation

Test Condition: Line and Load regulation are measured output voltage regulations according to changing input voltage and output load.

Table 7. Test Result

	85 V_{AC}	110 V_{AC}	230 V_{AC}	265 V_{AC}	350 V_{AC}	400 V_{AC}	460 V_{AC}
Full-Load	20.03 V	20.03 V	20.03 V	20.03 V	20.03 V	20.03 V	20.03 V
No-Load	20.04 V	20.04 V	20.04 V	20.04 V	20.04 V	20.04 V	20.04 V

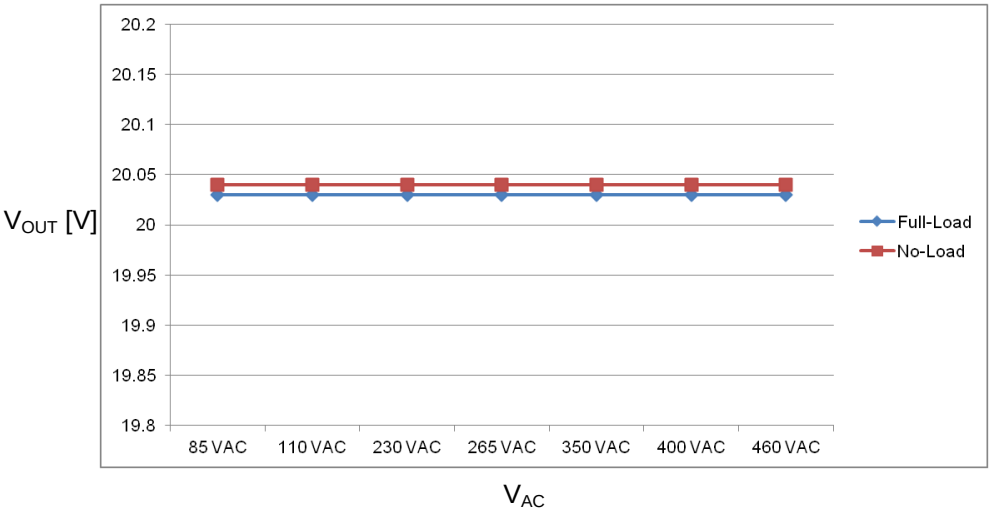

Figure 32. Line and Load Regulation

9.7. Hold-up Time

Test Condition: Measure the time interval between AC plug-out and V_{OUT} * 0.9. Load condition is 5% of full-load.

Table 8. Test Result

	85 V_{AC}	110 V_{AC}	230 V_{AC}	265 V_{AC}	350 V_{AC}	400 V_{AC}	460 V_{AC}
I_{OUT} = 15 mA	0.64 s	0.88 s	2.9 s	3.77 s	5.87 s	7.06 s	8.76 s

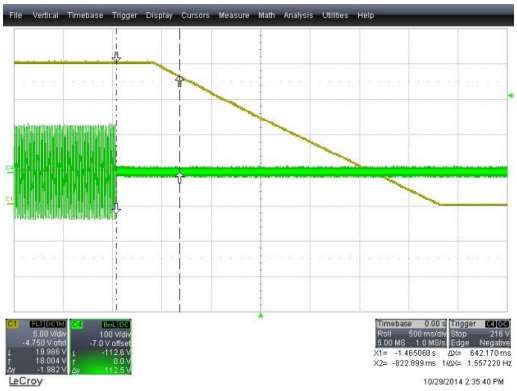

Figure 33. t_{HOLD} = 0.6 s, 85 V_{AC}, (CH1: V_{OUT} (5 V/div), CH4: V_{AC} (100 V/div), Time: 500 ms/div)

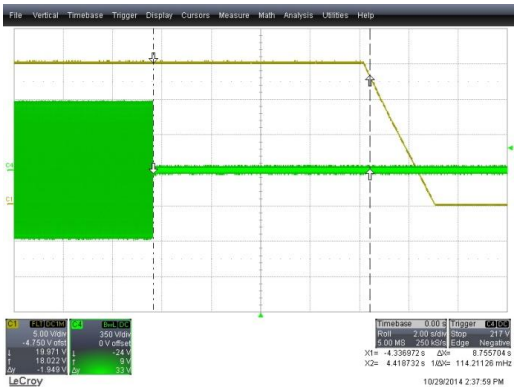

Figure 34. t_{HOLD} = 8.8 s, 460 V_{AC}, (CH1: V_{OUT} (5 V/div), CH4: V_{AC} (350 V/div), Time: 2 s/div)

9.8. Output Short Test

Test Condition: Measure “Hiccup” mode operation. Remove R108 because LOVP can be triggered over 400 V_{AC}.

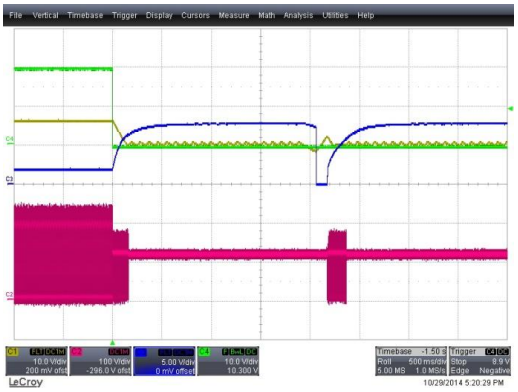

Figure 35. OLP Triggered, Output Short with 85 V_{AC}, Full-Load, (CH1: V_{CC} (10 V/div), CH2: V_{DS} (100 V/div), CH3: V_{FB} (5 V/div), CH4: V_{OUT} (10 V/div), Time: 500 ms/div)

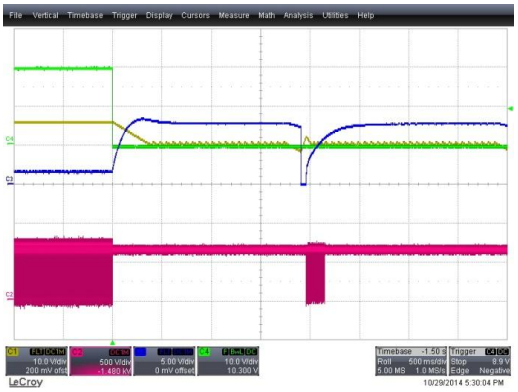

Figure 36. OLP Triggered, Output Short with 460 V_{AC}, Full-Load, (CH1: V_{CC} (10 V/div), CH2: V_{DS} (500 V/div), CH3: V_{FB} (5 V/div), CH4: V_{OUT} (10 V/div), Time: 500 ms/div)

9.9. Abnormal Over Current Test

Test Condition: Short secondary diode and measure “Hiccup” mode operation. Remove R108 because LOVP can be triggered over 400 V_{AC}.

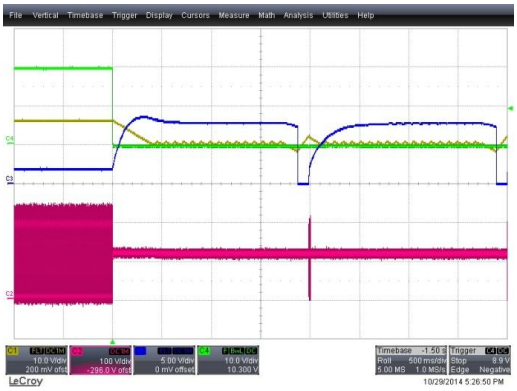

Figure 37. AOCP Triggered, Output Short with 85 V_{AC}, Full-Load, (CH1: V_{CC} (10 V/div), CH2: V_{DS} (100 V/div), CH3: V_{FB} (5 V/div), CH4: V_{OUT} (10 V/div), Time: 500 ms/div)

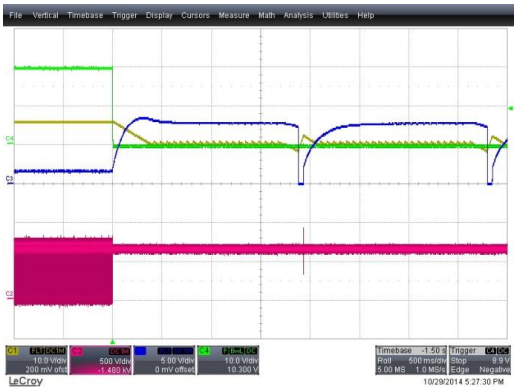

Figure 38. AOCP Triggered, Output Short with 460 V_{AC}, Full-Load, (CH1: V_{CC} (10 V/div), CH2: V_{DS} (500 V/div), CH3: V_{FB} (5 V/div), CH4: V_{OUT} (10 V/div), Time: 500 ms/div)

9.10. Efficiency

Test Condition: Measure the input and output power after 30 minutes aging.

Table 9. Test Results

	25% Load	50% Load	75% Load	Full-Load
85 V_{AC}	81.05%	84.20%	84.13%	83.97%
110 V_{AC}	80.71%	84.18%	84.82%	84.85%
230 V_{AC}	72.76%	80.34%	83.07%	83.71%
265 V_{AC}	70.25%	78.87%	82.20%	82.78%
350 V_{AC}	63.58%	74.59%	79.53%	80.29%
400 V_{AC}	59.52%	71.72%	77.61%	78.69%
460 V_{AC}	55.08%	68.13%	75.01%	76.60%

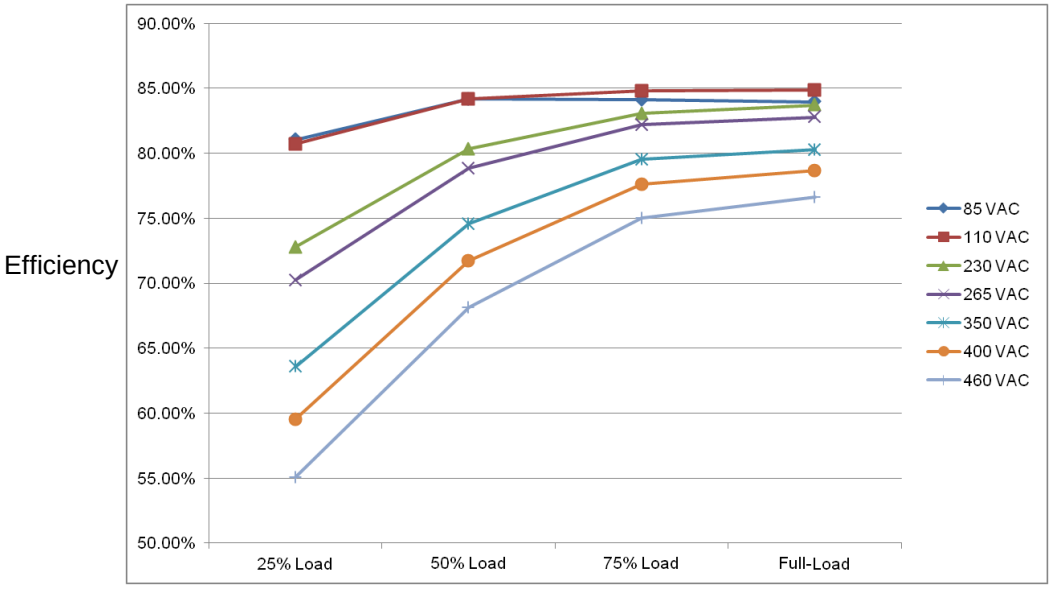

Figure 39. Efficiency Curve

9.11. Operating Temperature

Test Condition Measure the saturated temperature.

Table 10. Test Results

	85 V_{AC}	460 V_{AC}	Remark
FSL4110LRN	42.0°C	48.4°C	Box 2
Transformer	47.0°C	51.5°C	Circle 1
Secondary Rectifier with Snubber	41.8°C	49.0°C	Box 3

Temperature Photos

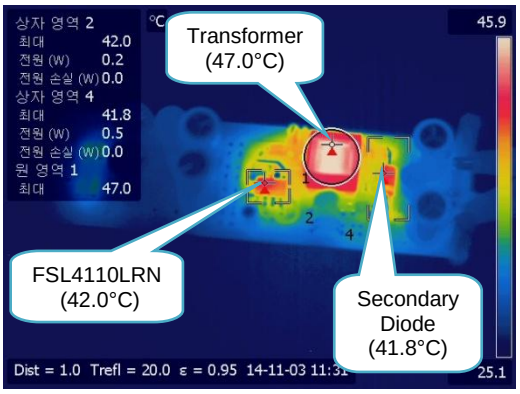

Figure 40. 85 V_{AC}; Top Side

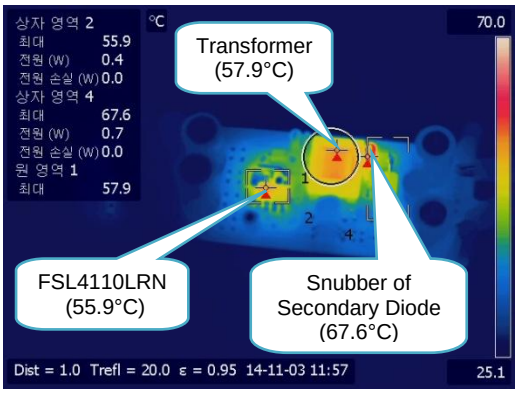

Figure 41. 460 V_{AC}; Top Side

9.12. Electromagnetic Interference (EMI)

Test Conditions:

- Frequency Subrange: 150 kHz – 30 MHz,
- Measuring: QuasiPeak; Average
- Load is 65.5 Ω Resistor

Table 11. Test Results

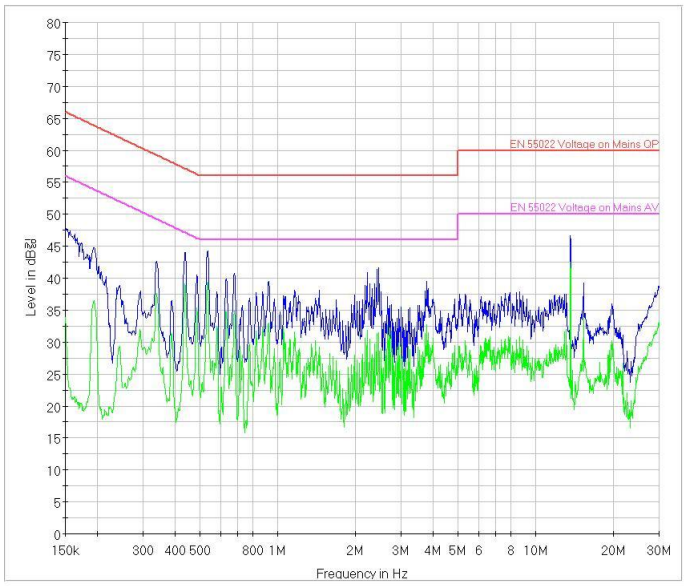

Figure 42. Conduction Line: 110 V_{AC}

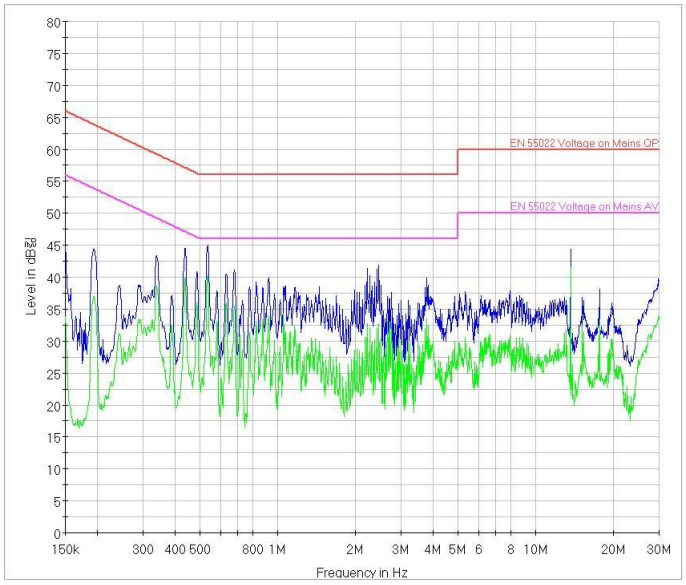

Figure 43. Conduction Neutral: 110 V_{AC}

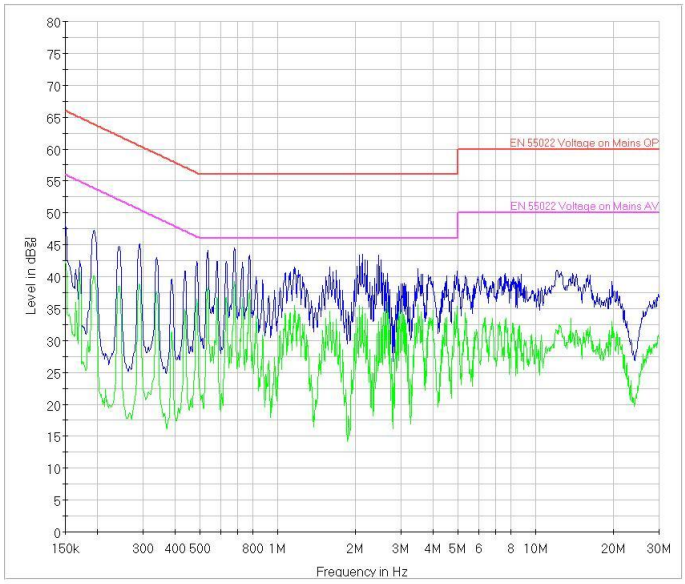

Figure 44. Conduction Line: 220 V_{AC}

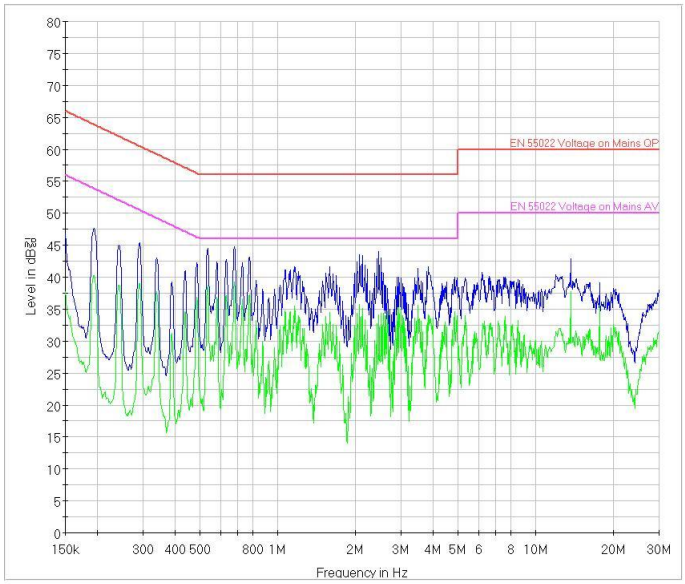

Figure 45. Conduction Neutral: 220 V_{AC}

10. Revision History

Rev.	Date	Description
1.0	Dec.16. 2014	Initial Release

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Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Users' Guide. Contact an authorized Fairchild representative with any questions.

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